Morgan Lewis
COUNSELORS AT LAW

Morgan, Lewis & Bockius LLP
1111 Pennsylvania Avenue, NW
Washington, DC 20004
Tel. 202.739.3000
Fax: 202.739.3001
www.morganlewis.com

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STATUTORY DECLARATION

I, Sun Suk KIM, a citizen of the Republic of Korea and a staff member of Y.H.KIM INTERNATIONAL PATENT & LAW OFFICE specializing in "ACTIVE MATRIX TYPE ORGANIC ELECTRO LUMINESCENCE DISPLAY PANEL AND METHOD OF FABRICATING THE SAME", do hereby declare that:

I am conversant with the English and Korean languages and a competent translator thereof.

To the best of my knowledge and belief, the following is a true and correct translation of the Priority Document (No. P2002-39475) in the Korean language already filed with Korean Industrial Property Office on July 8, 2002.

Signed this 23rd day February, 2005

Sun Suk KIM

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PATENT APPLICATION

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TITLE OF THE INVENTION: ACTIVE MATRIX TYPE ORGANIC ELECTRO LUMINESCENCE DISPLAY PANLE AND METHOD OF FABRICATING THE SAME

APPLICANT(S): LG. Philips LCD Co., Ltd.

ATTORNEY(S)

Young Ho KIM

INVENTOR(S)

Name: Chang Wook HAN

Address: #201, Ire House, 572-127, Seongsan-dong, Mapo-gu, Seoul, Korea

Nationality: Republic of Korea

The present application is filed pursuant to Article 42 of the Korea Patent Act.

Patent Attorney
Young Ho KIM

ABSTRACTS

[Abstract]

The present invention relates to an active matrix type organic electro luminescence display panel and a method of fabricating the same that is adaptive for extending life span as well as improving light emission efficiency.

An active matrix type organic electro luminescence display panel according to an embodiment of the present invention includes: a substrate having a defined light emission area; a low refractive thin film made of a low refractive material on the substrate and preventing a refraction of an emitted light; thin film transistors, formed on a predetermined location of the substrate having the low refraction thin film by a mask process having a photolithography method, switching and driving by a control signal from an exterior; a storage capacitor connected to the thin film transistor to charge/discharge a data signal from the exterior; and an organic electro luminescence diode patterned by the mask process of the thin film transistors to be formed on the substrate, which the light emission area is exposed, emitting light by an exterior current and voltage.

By above-mentioned compositions, the active matrix type organic electro luminescence display panel and the method of fabricating the same emits light emitted from the organic electro luminescence diode to a lower substrate and uses the low refractive material to improve a brightness and a light emission efficiency thereof.

[Representative drawing]

FIG. 4

SPECIFICATION

[Title of the invention]

ACTIVE MATRIX TYPE ORGANIC ELECTRO LUMINESCENCE DISPLAY PANEL AND METHOD OF FABRICATING THE SAME

[Brief description of the drawings]

FIG. 1 is a diagram representing a general basic pixel structure of an active matrix type organic EL display panel.

FIG. 2 is a sectional view representing an active matrix type organic EL display panel of the related art.

FIG. 3A to 3I are sectional views representing a fabricating method of the active matrix type organic EL display panel shown in FIG. 2 step by step.

FIG. 4 is a sectional view representing an active matrix type organic EL display panel according to a first embodiment of the present invention.

FIG. 5A to 5I are sectional views representing a fabricating method of the active matrix type organic EL display panel shown in FIG. 4 step by step.

FIG. 6 is a sectional view representing an active matrix type organic EL display panel according to a second embodiment of the present invention.

FIG. 7A to 7I are sectional views representing a fabricating method of the active matrix type organic EL display panel shown in FIG. 6 step by step.

FIG. 8 is a sectional view representing an active matrix type organic EL display panel according to a third embodiment of the present invention.

FIG. 9A to 9I are sectional views representing a fabricating method of the active matrix type organic EL display panel shown in FIG. 8 step by step.

<Detailed description of the reference numerals>

1 : an insulating substrate
30, 70 : a buffer layer
32, 72 : a semiconductor layer
32a, 72a : an active layer
32b, 72b : an ohmic contact layer
34, 74 : a capacitor electrode
36, 76 : a gate insulating film
38, 78 : a gate electrode
40, 44, 54, 80, 84, 94 : an insulating layer
42, 82 : a power electrode
46a, 46b, 86a, 86b : an ohmic contact hole
48, 88: a capacitor contact hole
56 : a drain contact hole

58, 98 : an anode electrode
60, 100 : a protective layer
62, 102 : an anode-exposed part
64, 104 : an organic electro luminescence(EL) layer
66, 106 : a cathode electrode
68 : a low refractive thin film

[Detailed description of the invention]
[Object of the invention]
[Technical field including the invention and prior art therein]

The present invention relates to an organic electro luminescence display panel, and more particularly, to an active matrix type organic electro luminescence display panel and a method of fabricating the same that is adaptive for extending life span as well as improving light emission efficiency.

Recently, there have been developed various flat panel displays with their weight and bulk reduced, which is the disadvantage of a cathode ray tube CRT. Such flat panel displays include a liquid crystal display LCD, a field emission display FED, a plasma display panel PDP, and an electro luminescence EL display panel.

There have been progressing active researches to try to increase the display quality of such flat panel displays and to make a screen large. The EL display panel between them is a self-luminous device emitting light by itself. The EL display panel excites fluorescent material in use of carriers such as electrons and holes etc to display a video image.

The EL display panel is generally classified into an inorganic EL display panel and an organic EL display panel in accordance with a used material. The organic EL display panel requires a high voltage of 100~200V and is driven with a voltage lower the inorganic EL display panel by 5~20V, so that it is possible to drive the organic EL display panel with a low DC voltage. Further, the organic EL display panel can be used as a flat panel display because it has excellent characteristics such as a wide viewing angle, a high-speed response time and a high contrast ratio etc, and the organic EL display is suitable for the next generation flat display because it is thin and light and has a good color impression.

On the other hand, there is mainly used a passive matrix organic EL display panel that does not include thin film transistors separately.

However, the passive matrix organic EL display panel is limited in resolution, power consumption and life span

etc, thus an active matrix organic EL display panel has been researched and developed in order to fabricate a next generation display that requires high resolution or large screen.

To describe this, in the passive matrix type, scan lines cross signal lines to form a device in a matrix, and the scan lines are sequentially driven in accordance with time to drive each pixel. Accordingly, an instantaneous brightness is required as much as a product of an average brightness and the number of lines in order to display a required average brightness. Accordingly, as there are more lines, a higher voltage and more current should be applied instantly, thus the device is rapidly deteriorated, power consumption is increased, so that it is not suitable for a high resolution and large-sized display.

Differently from this, in the active matrix type, a thin film transistor (hereinafter, referred to as TFT) opening and shutting each pixel is located at each pixel, the TFT acts as a switch, a first electrode connected to the TFT is turned on/off by the pixel, and a second electrode opposite to the first electrode is used as a common electrode. In such an active matrix organic EL display panel, the voltage applied to the pixel is charged to a storage capacitor Cst and the charged voltage in the storage capacitor acts to apply power source until the next frame signal is applied. Due to this, the organic EL display panel is driven for one frame period regardless of the number of gate lines, i.e., the number of scan lines.

Accordingly, the active matrix organic EL display panel has advantages in that low power consumption, high precision and large screen can be achieved because brightness is the same even though a low current is applied.

FIG. 1 is a diagram representing a general basic pixel structure of an active matrix organic EL display device.

Referring to FIG. 1, the basic pixel structure of the active matrix type organic EL display panel includes a scan line formed in a first direction; a power supply line and a signal line formed in parallel in a second direction crossing the first direction while being separated with a designated gap therebetween; and a pixel area covered by the scan line, the signal line and the power supply line.

Further, the basic pixel structure of the active matrix organic EL display panel includes a switching TFT formed at an intersection area of the scan line L and the signal line, a storage capacitor formed between the switching TFT and the power supply line, a drive TFT formed to be connected to the storage capacitor and the power supply line for acting a current source, and an

organic EL diode connected to the drive TFT.

The switching TFT controls a voltage and stores a current source.

In the organic EL diode, if an organic luminous material is supplied with a forward current, holes and electrons are moved to a light emission layer formed between a hole transport layer and an electron transport layer through a hole injection layer, the hole transport layer, the electron transport layer and an electron injection layer that are deposited between an anode electrode supplying holes and a cathode electrode supplying electrons. The moved holes and electrons are combined together within the light emission layer to generate a designated energy, which causes to emit light.

To describe the drive of the active matrix organic EL display panel through this configuration, if a signal is applied to a pertinent electrode in accordance with the selection signal, a gate of the switching TFT is in a turn-on state. At this moment, a data signal is applied to the drive TFT and the storage capacitor through the switching TFT. If the drive TFT is in the turn-on state, a current from the power supply line is applied to an organic EL layer through the drive TFT. In this case, the open and close time of a gate of the drive TFT becomes different in accordance with the size of the data signal, gray levels can be expressed by way of controlling the amount of current flowing through the drive TFT.

Also, the organic EL display panel can emit light continuously until the signal of the next frame is applied after a data charged in the storage capacitor is continuously applied to the drive TFT.

According to the driving principle, the active matrix organic EL display panel can apply the voltage lower and the current instantaneously lower than the passive matrix organic EL display panel, and the organic EL display panel can be continuously driven for one frame period regardless of the number of selected lines. Hereby, the active matrix organic EL display panel is advantageous for low power consumption, high resolution and a large screen. On the other hand, the active matrix organic EL display panel has a structure where a current flows through a TFT, a polycrystalline silicon p-Si TFT is required which has a uniform crystalline state so as for the electric field effect mobility to be excellent because the related art amorphous silicon a-Si TFT is difficult to be adopted because silicon particles of non-crystalline state of the amorphous silicon causes electric field effect mobility to be low.

The polycrystalline silicon TFT has high electric field effect mobility, thus a drive circuit can be made on

a substrate. Hereby, when the drive circuit is made on the substrate with the polycrystalline silicon TFT, the cost can be reduced and mounting of the drive integrated circuit IC can be simplified.

As a method of fabricating the polycrystalline silicon, there is mainly used a low temperature crystallization method by a laser annealing in use of amorphous silicon.

FIG. 2 is a sectional diagram of an active matrix organic EL display panel of the related art, explains an example of a drive TFT connected to an organic EL diode and a storage capacitor in FIG. 1, and represents an organic EL display panel of lower light emission method where an emitted light is transmitted through an anode of a lower electrode.

Referring to FIG. 2, the related art organic EL display panel includes a TFT T having a semiconductor layer 32, a gate electrode 38, source and drain electrodes 50 and 52 on an insulating substrate 1. The TFT T is connected to a storage capacitor Cst and an organic EL diode E.

The storage capacitor Cst includes a power electrode 42 and a capacitor electrode 34 that are opposite to each other with an insulating substance therebetween. The organic EL diode E includes an anode 58 and a cathode 66 that are opposite to each other with an organic EL layer 64 therebetween.

To be more specifically, a source electrode 50 of the TFT T is connected to the power electrode 42 and a drain electrode 52 is connected to the anode 58 that is a lower electrode of the organic EL diode E.

Generally, the anode 58 of a lower part light emission scheme, as above, is formed of a light transmitting material so as for the emitted light to be transmitted at the organic EL layer 64. The cathode 66 is formed of a metal with low work function so as for electrons to be injected smoothly into the organic EL layer 64.

However, in the organic EL display panel driven by the upper light emission scheme, the cathode 66 is formed of the light transmitting material because the light emitted from the organic EL layer 64 is transmitted upward through the cathode 66.

On the other hand, the organic EL display panel has a deposition structure of insulating layers where a buffer layer 30 buffing between the insulating substrate 1 and the semiconductor layer 32, a first insulating layer 40 to be an insulating substance for the storage capacitor Cst, a second insulating layer 44 between the source electrode 50 and the power electrode 42, a third insulating layer 54

between the anode 58 and the drain electrode 52, and a protective layer 60 between the anode 58 and the organic EL layer 64 are deposited one by one. The first to third insulating layers 40, 44, 54 and the protective layer 60 include a contact hole for connecting the layers electrically.

FIG. 3A to 3I are sectional views representing a fabricating method of the active matrix organic EL display panel shown in FIG. 2 step by step. Each pattern in such a fabricating method is formed by way of going through a series of processes where a pattern drawn in a separate mask is formed by way of being transferred to a substrate on which a thin film is deposited. Such processes are photolithography including photo-resist coating, aligning & exposure and developing.

Referring to FIG. 3A to 3I, the buffer layer 30, an active layer 32A and a capacitor electrode 34 are formed on the insulating substrate 1, as shown in FIG. 3A. At this moment, the buffer layer 30 is formed across the entire surface of the substrate in use of the first insulating material, the active layer 32a and the capacitor electrode 34 are formed by a first mask process after spreading on the entire surface of the upper part of the buffer layer 30 in use of polycrystalline silicon.

Then, a gate insulating film 36 and a gate electrode 38, as shown in FIG. 3B, are formed at the central area of the active layer 32a. The gate insulating film 36 and the gate electrode 38 are formed by a second mask process after continuously depositing a second insulating material and a first metal material on the substrate, as shown in FIG. 3A.

After forming the gate insulating film 36 and the gate electrode 38, an insulating layer 40 and a power electrode are formed on the insulating substrate 1, as shown in FIG. 3. The first insulating layer 40 is formed by way of spreading a third insulating material on the entire surface of the insulating substrate 1. The power electrode 42 is formed by way of patterning by a third mask process to cover the capacitor electrode 34 after depositing a second metal material on the upper part of the first insulating layer 40.

Then, as shown in FIG. 3D, a second insulating layer 44 is formed on the insulating substrate 1 in FIG. 3C. The second insulating layer 44 is formed by way of patterning by a fourth mask process after depositing a third insulating material on the entire surface of the insulating substrate 1 in FIG. 3. Then, the second insulating layer 44 has first and second ohmic contact holes 46a and 46b and a capacitor contact hole 48 to expose both ends of the active layer 32a and a part of the

power electrode 42. Herein, the both ends of the active layer 32a are connected through the first and second ohmic contact holes 46a and 46b and the source and drain electrodes formed in the following process. The left end of the active layer 32a becomes a drain area Ia, and the right end becomes a source area Ib.

The both exposed ends of the active layer 32a become the ohmic contact layer 32b that is ion-doped and contains impurities. Hereby, the semiconductor layer 32 is completed, which includes the active layer 32a and the ohmic contact layer 32b.

After completion of the semiconductor layer, as shown in FIG. 3E, the source and drain electrodes 50 and 52 are formed. The source and drain electrodes are formed by a fifth mask process after depositing a third metal material on the entire surface of the insulating substrate 1 shown in FIG. 3D. At this moment, the source electrode 50 is formed to be connected to the power electrode 42 and the ohmic contact layer 32b of the source area Ib through the first ohmic contact hole (46a of FIG. 3D) and the capacitor contract hole (48 of FIG. 3D), and the drain electrode 52 is formed to be connected to the ohmic contact layer 32b of the drain area Ia through the second ohmic contact hole (46b of FIG. 3D).

Through this process, the TFT T is completed, which includes the semiconductor layer 32, the gate electrode 38, the source and drain electrodes 50 and 52, and the storage capacitor Cst is formed at a corresponding area between the power electrode 42 and the capacitor electrode 34. Even though not shown in the drawings, the capacitor electrode 34 is connected to the gate electrode 38, the power electrode 42 is formed to be unified with the power supply line located to be parallel to the signal line.

Then, the third insulating layer 54 is formed as shown in FIG. 3F. The third insulating layer 54 is formed by way of patterning the drain contact hole 56 by a sixth mask process after depositing a fourth insulating material on the entire surface of the insulating substrate 1 shown in FIG. 3E.

Then, an anode 58 is formed on a light emission area I as shown in FIG. 3G. The anode 58 is formed by a seventh mask process in use of a transparent conductive material to be connected to the drain electrode 52 through the drain contact hole (56 of FIG. 3F).

Then a protective layer 60 is formed to have an anode-exposed part 62 as shown in FIG. 3H. The protective layer 60 is formed by way of patterning by an eighth mask process to expose a part of the anode 58 after depositing a fifth insulating material on the insulating substrate 1 shown in FIG. 3G. Herein, the protective layer 60 acts to

protect the TFT T from moisture and impurities.

Hereby, the mask process including the photolithography is completed, an organic EL layer 64 and a cathode 66 are sequentially formed, which forms an organic EL diode E along with the anode 58 through the anode-exposed part (62 of FIG. 3H) as shown in FIG. 3I.

However, in case that the organic EL display panel is of a lower light emission scheme where a light emitted in the organic EL layer 64 comes out toward the substrate 1, there is a disadvantage in that a light transmittance is deteriorated by the first to third insulating layers 40, 44 and 54 and the buffer layer 30 formed when fabricating a TFT T array, i.e., inorganic insulating films such as silicon nitride SiNx and silicon oxide SiOx.

Further, the organic EL display panel of the related art emits light to the outside through a plurality of insulating layer, thus there is a disadvantage in that light emission efficiency, i.e., quantum efficiency, is low. This can be known through Formula 1 that calculates light emission efficiency on the basis of classical optics.

[Formula 1]

$$\eta_{ext} = \frac{1}{2n^2} \times \eta_{int} = \frac{1}{2 \times 1.5^2} = \frac{1}{5} \approx 20\%$$

Herein, 'η' represents internal or external light emission efficiency, and 'n' represents the refractive rate of a pertinent substrate. The refractive rate n of a substrate on which a buffer layer and an insulating layer are deposited in the related art is 1.5.

Hereby, in the organic EL display panel according to the related art, there is a disadvantage in that only 20% of the light emitted from the organic EL layer 64 to be transmitted through the substrate 1 is utilized on the display panel.

[Technical Subject Matter to be solved by the Invention]

Accordingly, it is an object of the present invention to provide an active matrix type organic electro luminescence display panel and a method of fabricating the same that is adaptive for improving a brightness and light emission efficiency thereof.

[Configuration and Operation of the Invention]

In order to achieve these and other objects of the invention an active matrix organic electro luminescence display panel according to an aspect of the present invention includes: a substrate having a defined light

emission area; a low refractive thin film, made of a low refractive material on the substrate, reducing a loss of light; thin film transistors, formed on a predetermined location of the substrate having the low refraction thin film by a mask process having a photolithography method, switching and driving by a control signal from an exterior; a storage capacitor connected to the thin film transistor to charge/discharge a data signal from the exterior; and an organic electro luminescence diode patterned by the mask process of the thin film transistors to be formed on the substrate, which the light emission area is exposed, emitting light by an exterior current and voltage.

The low refractive thin film is patterned by the mask process of the thin film transistors to expose the substrate having the light emission area, and then is included in between the insulated substrate and the organic electro luminescence diode.

An active matrix type organic electro luminescence display panel includes: a substrate having a defined light emission area; a low refractive thin film formed by applying a low refractive material to the substrate in order to reduce a loss of the emitting light; thin film transistors, formed on a predetermined location of the substrate by a mask process having a photolithography method, switching and driving by a control signal from an exterior; a storage capacitor connected to the thin film transistor to charge/discharge a data signal from the exterior; and an organic electro luminescence diode formed on the light emission area of the substrate having the thin film transistor and the storage capacitor, and emitting light by an external current and a voltage.

The low refractive material has a refractive rate (n) less than 1.5.

The low refractive material includes silica aerogel and silica gel, which have a refractive rate (n) less than 1.5.

The organic electro luminescence diode includes: a first electrode formed of a transparent conductive material on the light emission area of the substrate; an organic light emission layer formed of an organic light emission material on the light emission area of the substrate to cover the first electrode; and a second electrode formed of a metal material on an upper part of the organic light emission layer to coat the entire surface of the substrate.

The thin film transistors include: a semiconductor layer formed on the substrate; a gate insulating film and a gate electrode stacked sequentially on an upper part of the semiconductor layer; a drain electrode formed to be

connected to the semiconductor layer and the first electrode of the organic electro luminescence diode; and a source electrode simultaneously formed together with the drain electrode to be connected to the semiconductor layer and the storage capacitor.

The storage capacitor includes: a capacitor electrode separated from the semiconductor layer by a predetermined distance on the substrate; and a power electrode insulated from an upper part of the capacitor electrode and then connected to the source electrode, as well as, formed to cover the capacitor electrode.

The semiconductor layer is a P type semiconductor layer, and the first and the second electrodes are an anode and a cathode, respectively.

The transparent conductive material includes indium-tin-oxide (ITO).

A method of fabricating an active matrix type organic electro luminescence display panel includes: forming a low refractive thin film by applying a low refractive material on the entire surface of a substrate having a defined light emission area; forming a buffer layer on the substrate having the low refractive thin film by way of a mask process to reveal the light emission area on the substrate; forming an active layer and a capacitor electrode separated by a predetermined distance from each other on the buffer layer by way of a mask process having exposing, developing, and etching; sequentially forming a gate insulating film and a gate electrode at a central part of the active layer; forming a first insulating layer on the entire surface of the substrate to cover the gate insulating film and the gate electrode; forming a power electrode on the substrate to cover an area corresponding to the capacitor electrode of the first insulating layer;

forming a second insulating layer on the entire surface of the substrate to cover the power electrode; exposing the substrate onto which the low refractive thin film on a predetermined area of the active layer and the power electrode and the light emission area is coated; ion doping the substrate having the exposed active layer to complete a semiconductor layer; forming a source electrode and a drain electrode separated by a predetermined distance from each other through a predetermined area of the semiconductor layer and the power electrode; forming a third insulating layer to cover the source and the drain electrodes; forming a drain contact hole and patterning the third insulating layer to expose the substrate onto which the low refractive thin film of the light emission area is coated; and forming an organic electro luminescence diode connected to the drain electrode on the substrate, which the exposed low

refractive thin film of the light emission area is coated.

The forming the organic electrode luminescence diode includes: forming a first electrode made of a transparent conductive material on the emission area having the substrate onto which the exposed low refractive thin film is coated; applying an organic light emission material to the light emission area having the first electrode to form an organic light emission layer; and forming a second electrode made of a metal material on the entire surface of the substrate to apply an electrical signal to the organic light emission layer together with the first electrode.

The method further includes forming a protective layer, which a light emission part of the first electrode is exposed, after forming the first electrode.

The semiconductor layer is a P type semiconductor layer doped by a P type ion, and the first and the second electrode are respectively an anode and a cathode.

A method for fabricating an active matrix type organic luminescence display panel includes: forming a buffer layer on the substrate having a defined light emission area by way of a mask process to reveal the light emission area; forming an active layer and a capacitor electrode separated by a predetermined distance from each other on the buffer layer by way of a mask process having exposing, developing, and etching; sequentially forming a gate insulating film and a gate electrode at a central part of the active layer; forming a first insulating layer on the entire surface of the substrate to cover the gate insulating film and the gate electrode; forming a power electrode on the substrate to cover an area corresponding to the capacitor electrode of the first insulating layer; forming a second insulating layer on the entire surface of the substrate to cover the power electrode; exposing the substrate onto which the low refractive thin film on a predetermined area of the active layer and the power electrode and the light emission area is coated; ion-doping the substrate having the exposed active layer to complete a semiconductor layer; forming a source electrode and a drain electrode separated by a predetermined distance from each other through a predetermined area of the semiconductor layer and the power electrode; sequentially forming a third insulating layer and a low refractive thin film to cover the source and the drain electrodes; patterning the third insulating layer and the low refractive thin film so as to form a drain contact hole; and forming an organic electro luminescence diode connected to the drain electrode on the substrate, which the exposed low refractive thin film of the light emission area is coated.

A method of fabricating an active matrix type organic electro luminescence display panel includes: forming a low refractive thin film by applying a low refractive material to the entire surface of a substrate having a defined light emission area; forming a buffer layer on the entire surface of the substrate having the low refractive thin film; forming an active layer and a capacitor electrode separated by a predetermined distance from each other on the buffer layer by way of a mask process having exposing, developing, and etching; sequentially forming a gate insulating film and a gate electrode at a central part of the active layer; forming a first insulating layer on the entire surface of the substrate to cover the gate insulating film and the gate electrode; forming a power electrode on the substrate to cover an area corresponding to the capacitor electrode of the first insulating layer; forming a second insulating layer on the entire surface of the substrate to cover the power electrode; exposing a predetermined area of the active layer and the power electrode; ion-doping the substrate having the exposed active layer to complete a semiconductor layer; forming a source electrode and a drain electrode separated by a predetermined distance from each other through a predetermined area of the semiconductor layer and the power electrode; forming a third insulating layer to cover the source and the drain electrodes; patterning the third insulating layer so as to form a drain contact hole; and forming an organic electro luminescence diode on the substrate so as to connect to the drain electrode.

The forming the organic electrode luminescence diode includes: forming a first electrode of a transparent conductive material on the emission area having the substrate to which the low refractive thin film, the buffer layer, and the first to the third insulating layer are sequentially stacked; applying an organic light emission material to the light emission area of the substrate having the first electrode to form an organic light emission layer; and forming a second electrode of a metal material on the entire surface of the substrate to apply an electrical signal to the organic light emission layer together with the first electrode.

These and other objects of the invention will be apparent from the following detailed description of the embodiments of the present invention with reference to the accompanying drawings.

Hereinafter, the preferred embodiments of the present invention will be described in detail with reference to FIGs. 4 to 9I.

A basic pixel structure of an active matrix organic EL display panel according to an embodiment of the present

invention can has the same configuration and effect. and driven in the same way as that of FIG. 1.

FIG. 4 is a sectional view representing an active matrix organic EL display panel according to a first embodiment of the present invention, wherein a drive TFT connected to a storage capacitor and an organic EL diode in FIG. 1 is described as an example, the organic EL display panel is of a lower light emission scheme where an emitted light is transmitted through an anode of lower electrode to be radiated.

Referring to FIG. 4, the organic EL display panel according to the first embodiment of the present invention includes an insulating substrate 1 with a low refractive thin film 68 spread on the entire surface thereof; a TFT T having a semiconductor layer 72, a gate electrode 78 and source and drain electrodes 90 and 92 on a buffer layer 70 provided on the insulating substrate 1; and a storage capacitor Cst and an organic EL diode E connected to the TFT T.

The low refractive thin film 68 is for utilizing more light emitted from the organic EL diode E on the display panel. The low refractive thin film 68 is formed of a material with low refractive rate such as silica aerogel and silica gel. Herein, the refractive rate n of silica aerogel is 1.07.

The TFT T is connected to the storage capacitor Cst and the organic EL diode E to be driven when the gate signal is enabled. Hereby, the organic EL diode E generates the light corresponding to the size of the pixel signal across the data line DL.

The storage capacitor Cst includes a power electrode 82 and a capacitor electrode 74 that are opposite to each other with an insulating substance therebetween. The organic EL diode E includes an anode 98 and a cathode 106 that are opposite to each other with an organic EL layer 104 therebetween.

To be more specifically, a source electrode 90 of the TFT T is connected to the power electrode 82 and a drain electrode 92 is connected to the anode 98 that is a lower electrode of the organic EL diode E.

Generally, the anode 98 of a lower part light emission scheme, as above, is formed of a light transmitting material so as for the emitted light to be transmitted at the organic EL layer 104. The cathode 106 is formed of a metal with low work function so as for electrons to be injected smoothly into the organic EL layer 104.

On the other hand, a TFT T of the organic EL display panel has a deposition structure of insulating layers where a buffer layer 70 butting between the insulating

substrate 1, on which the low refractive film 68 is spread, and the semiconductor layer 72; a first insulating layer 80 to be an insulating substance for the storage capacitor CsL; a second insulating layer 84 between the source electrode 90 and the power electrode 82; a third insulating layer 94 between the anode 98 and the drain electrode 92; and a protective layer 100 between the anode 98 and the organic EL layer 104 are deposited one by one. The first to third insulating layers 80, 84, 94 and the protective layer 100 include a contact hole for connecting the layers electrically.

Differently, only organic EL diode E is formed in a light emission area T of the organic EL display panel without the buffer and insulating layers. The organic EL diode E includes an anode 98 formed of a transparent conductive material, a cathode 106 formed of a metal material, and an organic EL layer 104 formed between the anode 98 and the cathode 106. The organic EL layer 104 includes a hole injection layer, a hole transport layer, an electron transport layer and an electron injection layer that are sequentially deposited between the anode 98 and the cathode 106. Looking at its light emission principle, if a current is applied between the anode 98 and the cathode 106, carriers including electrons and holes are injected though the hole injection layer and the electron injection layer. Such carriers are transported to a light emission layer (not shown) formed between the hole transport layer and the electron transport layer through the hole transport layer and the electron transport layer. At this moment, the hole transport layer and the electron transport layer transport the carriers to a light emission material to increase a probability of light emission combination within the light emission layer. If the carriers are injected, excitons are generated within the light emission layer, and the generated excitons emit the light corresponding to a polaron energy gap to become extinct. Herein, the generated light is radiated toward the insulating substrate 1, i. e., a lower direction.

In the organic EL display panel with such a configuration, the light emitted from the light emission layer of the organic EL layer 104 is radiated to the outside through the substrate 1 without going through the insulating layer, i.e., displayed on the display screen, to improve a brightness and a brightness uniformity, and the light is not dispersed, because of going through the low refractive thin film 68, but utilized more on the display screen to improve a light emission efficiency.

For example, the refractive rate of silica aerogel is about 1.07, thus the light emitted from the organic EL layer 104 on the display screen can be known to improve by

Formula 2.

[Formula 2]

$$\eta_{total} = \frac{1}{2n^2} \times \eta_{int} = \frac{1}{2 \times 1.07^2} \approx \frac{1}{2 \times 1^2} = \frac{1}{2} = 50\%$$

Hereby, the organic EL display panel according to the embodiment of the present invention eliminates the buffer layer and the insulating layer on the light emission area as well as forming the low refractive thin film 68, so that the light emission efficiency can be improved about 2.5 times more than the related art.

FIG. 5A to 5J are sectional diagrams representing a fabricating method of the active matrix organic EL display panel shown in FIG. 4 step by step. Each pattern in such a fabricating method is formed by way of going through a series of processes where a pattern drawn in a separate mask is formed by way of being transferred to a substrate on which a thin film is deposited. Such processes are photolithography including photo-resist coating, aligning & exposure and developing.

Referring to FIG. 5A to 5I, a low refractive thin film 68 is formed on the entire surface of an insulating substrate 1 as shown in FIG. 5A. The low refractive thin film 68 reduces the rate that the light generated from the organic EL diode E is refracted, thus the efficiency of the light emitted from the lower surface of the insulating substrate 1 is improved. Such a low refractive thin film 68 is formed of a material with low refractive rate, e.g., mainly silica aerogel and silica gel.

Then, the buffer layer 70, an active layer 72a and a capacitor electrode 74 are formed, as shown in FIG. 5B. At this moment, the buffer layer 70 is formed across the entire surface of the insulating substrate 1 with the low refractive thin film 68 spread on it in use of the first insulating material, then is patterned by a first mask process to leave an area except a light emission area I. The active layer 72a and the capacitor electrode 74 are formed by a second mask process after spreading polycrystalline silicon on the entire surface of the upper part of the buffer layer 70.

Then, a gate insulating film 76 and a gate electrode 78, as shown in FIG. 5C, are formed at the central area of the active layer 72a. The gate insulating film 76 and the gate electrode 78 are formed by a third mask process after continuously depositing a second insulating material and a first metal material on the insulating substrate 1, as shown in FIG. 5B.

After forming the gate insulating film 76 and the gate electrode 78, as shown in FIG. 5D, an insulating layer 80 and a power electrode 82 are formed on the insulating substrate 1. The first insulating layer 80 is formed by way of spreading a third insulating material on the entire surface of the insulating substrate 1 shown in FIG 5C. The power electrode 82 is formed by way of patterning by a fourth mask process to cover the capacitor electrode 74 after depositing a second metal material on the upper part of the first insulating layer 80.

Then, a second insulating layer 84, as shown in FIG. 5E, is formed on the insulating substrate 1 shown in FIG 5D. The second insulating layer 84 is formed by way of patterning by a fifth mask process after depositing a third insulating material on the entire surface of the insulating substrate 1 shown in FIG 5D. Then, the first and second insulating layers 80 and 84 are patterned for first and second ohmic contact holes 86a and 86b and a capacitor contact hole 88 to expose both ends of the active layer 72a and a part of the power electrode 82 and, in addition, for the insulating substrate 1 of the light emission area I to reveal itself. In this case, the patterning of the first and second insulating layers 80 and 84 is carried out at the same time when the first and second ohmic contact hole 86a and 86b and the capacitor contact hole 88, so that the light emission area I can be revealed.

Herein, both ends of the active layer 72a are connected through the first and second ohmic contact holes 86a and 86b and the source and drain electrodes formed in the following process. The left end of the active layer 72a becomes a drain area Ia, and the right end becomes a source area Ib.

The both exposed ends of the active layer 72a are ion-doped to become the ohmic contact layer 72b containing contains impurities. Hereby, the semiconductor layer 72 is completed, which includes the active layer 72a and the ohmic contact layer 72b.

After completion of the semiconductor layer 72, as shown in FIG. 5F, the source and drain electrodes 90 and 92 are formed. The source and drain electrodes are formed by a sixth mask process after depositing a third metal material on the entire surface of the insulating substrate 1 shown in FIG. 5E. At this moment, the source electrode 90 is formed to be connected to the power electrode 82 and the ohmic contact layer 72b of the source area Ib through the first ohmic contact hole (86a of FIG. 5E) and the capacitor contract hole (88 of FIG. 5E), and the drain electrode 92 is formed to be connected to the ohmic contact layer 72b of the drain area Ia through the second

ohmic contact hole (86b of FIG. 5E).

Through this process, the TFT T is completed, which includes the semiconductor layer 72, the gate electrode 78, the source and drain electrodes 90 and 92, and the storage capacitor Cst is formed at a corresponding area between the power electrode 82 and the capacitor electrode 74. Even though not shown in the drawings, the capacitor electrode 74 is connected to the gate electrode 78, the power electrode 82 is formed to be unified with the power supply line located to be parallel to the signal line.

Then, the third insulating layer 94 is formed as shown in FIG. 5G. The third insulating layer 94 is formed by way of patterning by a seventh mask process to expose the drain contact hole 96 and the light emission area I after depositing a fourth insulating material on the entire surface of the insulating substrate 1 shown in FIG. 5F.

Then, an anode 98, as shown in FIG. 5H, is formed on the light emission area I. The anode 98 is formed by an eighth mask process in use of a transparent conductive material to be connected to the drain electrode 92 through the drain contact hole (96 of FIG. 5G). Hereby, only the anode 98 is formed on the substrate 1 of the light emission area I through the above process.

Then a protective layer 100 is formed to have an anode-exposed part 102 as shown in FIG. 5I. The protective layer 100 is formed by way of patterning by a ninth mask process to expose a part of the anode 98 after depositing a fifth insulating material on the insulating substrate 1 shown in FIG. 5H. Herein, the protective layer 100 acts to protect the TFT T from moisture and impurities.

Hereby, the mask process including the photolithography is completed, an organic EL layer 104 and a cathode 106 are sequentially formed, which forms an organic EL diode E along with the anode 98 through the anode-exposed part (102 of FIG. 5I) as shown in FIG. 5J.

FIG. 6 is a sectional view representing an active matrix organic EL display panel according to a second embodiment of the present invention, wherein it is characterized in that the low refractive thin film 68 is located between the third insulating layer 94 and the anode 98 in comparison with FIG. 4 of the first embodiment of the present invention.

Referring to FIG. 6, the organic EL display panel according to the second embodiment of the present invention includes an insulating substrate 1 with a buffer layer 70 on top thereof; a TFT T having a semiconductor layer 72, a gate electrode 78 and source and drain electrodes 90 and 92 on the insulating substrate 1; and a

storage capacitor Cst and an organic EL diode E connected to the TFT T. Further, the organic EL display panel according to the second embodiment of the present invention has a low refractive thin film 68 formed between an organic EL diode E and an insulating layer 94 that is formed on a TFT T.

The TFT T is connected to the storage capacitor Cst and the organic EL diode E to be driven when the gate signal is enabled. Hereby, the organic EL diode E generates the light corresponding to the size of the pixel signal across the data line DL.

The storage capacitor Cst includes a power electrode 82 and a capacitor electrode 74 that are opposite to each other with an insulating substance therebetween. The organic EL diode E includes an anode 98 and a cathode 106 that are opposite to each other with an organic EL layer 104 therebetween.

To be more specifically, a source electrode 90 of the TFT T is connected to the power electrode 82 and a drain electrode 92 is connected to the anode 98 that is a lower electrode of the organic EL diode E.

Generally, the anode 98 of a lower part light emission scheme, as above, is formed of a light transmitting material so as for the emitted light to be transmitted at the organic EL layer 104. The cathode 106 is formed of a metal with low work function so as for electrons to be injected smoothly into the organic EL layer 104.

On the other hand, a TFT T of the organic EL display panel has a deposition structure of insulating layers where a buffer layer 70 buffing between the insulating substrate 1 and the semiconductor layer 72; a first insulating layer 80 to be an insulating substance for the storage capacitor Cst; a second insulating layer 84 between the source electrode 90 and the power electrode 82; a third insulating layer 94 between the anode 98 and the drain electrode 92; and a protective layer 100 between the anodo 98 and the organic EL layer 104 are deposited one by one. The first to third insulating layers 80, 84, 94 and the protective layer 100 include a contact hole for connecting the layers electrically.

Differently, in a light emission area T of the organic EL display panel, the organic EL diode E is formed on a third insulating layer 94 spread on the entire surface of the substrate after completion of the TFT T. The organic EL diode E includes an anode 98 formed of a transparent conductive material, a cathode 106 formed of a metal material, and an organic EL layer 104 formed between the anode 98 and the cathode 106. The organic EL layer 104 includes a hole injection layer, a hole transport layer,

an electron transport layer and an electron injection layer that are sequentially deposited between the anode 98 and the cathode 106. Looking at its light emission principle, if a current is applied between the anode 98 and the cathode 106, carriers including electrons and holes are injected though the hole injection layer and the electron injection layer. Such carriers are transported to a light emission layer (not shown) formed between the hole transport layer and the electron transport layer through the hole transport layer and the electron transport layer. At this moment, the hole transport layer and the electron transport layer transport the carriers to a light emission material to increase a probability of light emission combination within the light emission layer. If the carriers are injected, excitons are generated within the light emission layer, and the generated excitons emit the light corresponding to a polaron energy gap to become extinct. Herein, the generated light is radiated toward the insulating substrate 1 through the low refractive thin film 68 and the third insulating layer 94.

In the organic EL display panel with such a configuration, the light emitted from the light emission layer of the organic EL layer 104 is radiated not through the buffer layer 70 and the first and second insulating layer 80 and 04, but through the third insulating layer 94 and the insulating substrate 1, thus a light emission efficiency is improved as well as a brightness.

FIG. 7A to 7I are sectional diagrams representing a fabricating method of the active matrix organic EL display panel shown in FIG. 6 step by step. Each pattern in such a fabricating method is formed by way of going through a series of processes where a pattern drawn in a separate mask is formed by way of being transferred to a substrate on which a thin film is deposited. Such processes are photolithography including photo-resist coating, aligning & exposure and developing.

Referring to FIG. 7A to 7I, a buffer layer 70, an active layer 72a and a capacitor electrode 74, as shown in FIG. 7A, are formed on an insulating substrate 1. At this moment, the buffer layer 70 is formed across the entire surface of the insulating substrate 1 in use of the first insulating material, then is patterned by a first mask process to leave an area except a light emission area I. The active layer 72a and the capacitor electrode 74 are formed by a second mask process after spreading polycrystalline silicon on the entire surface of the upper part of the buffer layer 70.

Then, a gate insulating film 76 and a gate electrode 78, as shown in FIG. 7B, are formed at the central area of the active layer 72a. The gate insulating film 76 and the

gate electrode 78 are formed by a third mask process after continuously depositing a second insulating material and a first metal material on the insulating substrate 1, as shown in FIG. 7A.

After forming the gate insulating film 76 and the gate electrode 78, as shown in FIG. 7C, an insulating layer 80 and a power electrode 82 are formed on the insulating substrate 1. The first insulating layer 80 is formed by way of spreading a third insulating material on the entire surface of the insulating substrate 1 shown in FIG 7B. The power electrode 82 is formed by way of patterning by a fourth mask process to cover the capacitor electrode 74 after depositing a second metal material on the upper part of the first insulating layer 80.

Then, a second insulating layer 84, as shown in FIG. 7D, is formed. The second insulating layer 84 is formed by way of patterning by a fifth mask process after depositing a third insulating material on the insulating substrate 1 shown in FIG 7C. Then, the first and second insulating layers 80 and 84 are patterned for first and second ohmic contact holes 86a and 86b and a capacitor contact hole 88 to expose both ends of the active layer 72a and a part of the power electrode 82 and, in addition, for the insulating substrate 1 of the light emission area I to reveal itself. In this case, the patterning of the first and second insulating layers 80 and 84 is carried out at the same time when the first and second ohmic contact hole 86a and 86b and the capacitor contact hole 88, so that the light emission area I can be revealed.

Hereon, both ends of the active layer 72a are connected through the first and second ohmic contact holes 86a and 86b and the source and drain electrodes formed in the following process. The left end of the active layer 72a becomes a drain area Ia, and the right end becomes a source area Ib.

The both exposed ends of the active layer 72a are ion-doped to become the ohmic contact layer 72b containing contains impurities. Hereby, the semiconductor layer 72 is completed, which includes the active layer 72a and the ohmic contact layer 72b.

After completion of the semiconductor layer 72, as shown in FIG. 7E, the source and drain electrodes 90 and 92 are formed. The source and drain electrodes are formed by a sixth mask process after depositing a third metal material on the entire surface of the insulating substrate 1 shown in FIG. 7D. At this moment, the source electrode 90 is formed to be connected to the power electrode 82 and the ohmic contact layer 72b of the source area Ib through the first ohmic contact hole (86a of FIG. 7D) and the capacitor contract hole (88 of FIG. 7D), and the drain

electrode 92 is formed to be connected to the ohmic contact layer 72b of the drain area 1a through the second ohmic contact hole (86b of FIG. 7D).

Through this process, the TFT T is completed, which includes the semiconductor layer 72, the gate electrode 78, the source and drain electrodes 90 and 92, and the storage capacitor Cst is formed at a corresponding area between the power electrode 82 and the capacitor electrode 74. Even though not shown in the drawings, the capacitor electrode 74 is connected to the gate electrode 78, the power electrode 82 is formed to be unified with the power supply line located to be parallel to the signal line.

Then, the third insulating layer 94 and the low refractive thin film 68 are sequentially formed as shown in FIG. 7E. The third insulating layer 94 and the low refractive thin film 68 are formed by way of patterning by a seventh mask process to form the drain contact hole 96 after depositing a fourth insulating material and a low refractive material respectively on the entire surface of the insulating substrate 1 shown in FIG. 7E.

Then, an anode 58, as shown in FIG. 7G, is formed on the light emission area I. The anode 58 is formed by an eighth mask process in use of a transparent conductive material to be connected to the drain electrode 92 through the drain contact hole (96 of FIG. 7F). Hereby, the third insulating layer 94, the low refractive thin film 68 and the anode 98 are configured in a state of being sequentially deposited on the substrate 1 of the light emission area I through the above process.

Then a protective layer 100 is formed to have an anode-exposed part 102 as shown in FIG. 7H. The protective layer 100 is formed by way of patterning by a ninth mask process to expose a part of the anode 98 after depositing a fifth insulating material on the insulating substrate 1 shown in FIG. 7G. Herein, the protective layer 100 acts to protect the TFT T from moisture and impurities.

Hereby, the mask process including the photolithography is completed, an organic EL layer 104 and a cathode 106 are sequentially formed, which forms an organic EL diode E along with the anode 98 through the anode exposed part (102 of FIG. 7H) as shown in FIG. 7I.

FIG. 8 is a sectional view representing an active matrix organic EL display panel according to a third embodiment of the present invention, wherein it is characterized in that the low refractive thin film 68 is located between the substrate 1 and the buffer layer 70 in comparison with the organic EL display panel of the related art shown in FIG. 2.

Referring to FIG. 8, the organic EL display panel according to the third embodiment of the present invention

includes an insulating substrate 1 with a low refractive thin film 68 spread on the entire surface thereof; a TFT T having a semiconductor layer 72, a gate electrode 78 and source and drain electrodes 90 and 92 on a buffer layer 70 provided on the insulating substrate 1; and a storage capacitor Cst and an organic EL diode E connected to the TFT T. Further, the organic EL display panel according to the third embodiment of the present invention has a low refractive thin film 68 formed between an organic EL diode E and an insulating layer 94 that is formed on a TFT T.

The TFT T is connected to the storage capacitor Cst and the organic EL diode E to be driven when the gate signal is enabled. Hereby, the organic EL diode E generates the light corresponding to the size of the pixel signal across the data line DL.

The storage capacitor Cst includes a power electrode 82 and a capacitor electrode 74 that are opposite to each other with an insulating substance therebetween. The organic EL diode E includes an anode 98 and a cathode 106 that are opposite to each other with an organic EL layer 104 therebetween. At this time, the organic EL diode is formed in a state being deposited on the insulating substrate 1 having a defined light emission area.

To be more specifically, a source electrode 90 of the TFT T is connected to the power electrode 82 and a drain electrode 92 is connected to the anode 98 that is a lower electrode of the organic EL diode E.

Generally, the anode 98 of a lower panel light emission scheme, as above, is formed of a light transmitting material so as for the emitted light to be transmitted at the organic EL layer 104. The cathode 106 is formed of a metal with low work function so as for electrons to be injected smoothly into the organic EL layer 104.

On the other hand, a TFT T and a light emission area I of the organic EL display panel has a deposition structure of insulating layers where a buffer layer 70 butting between the insulating substrate 1, on which the low refractive film 68 is spread, and the semiconductor layer 72; a first insulating layer 80 to be an insulating substance for the storage capacitor Cst; a second insulating layer 84 between the source electrode 90 and the power electrode 82; a third insulating layer 94 between the anode 98 and the drain electrode 92; and a protective layer 100 between the anode 98 and the organic EL layer 104 are deposited one by one. The first to third insulating layers 80, 84, 94 and the protective layer 100 include a contact hole for connecting the layers electrically.

Further, the light emission area I of the organic EL

display panel includes a buffer layer 70, first to third insulating layers 80, 84 and 94, and an organic EL diode E that are sequentially deposited on the substrate 1 with the low refractive thin film 68 spread thereon. The organic EL diode E includes an anode 98 formed of a transparent conductive material, a cathode 106 formed of a metal material, and an organic EL layer 104 formed between the anode 98 and the cathode 106. The organic EL layer 104 includes a hole injection layer, a hole transport layer, an electron transport layer and an electron injection layer that are sequentially deposited between the anode 98 and the cathode 106. Looking at its light emission principle, if a current is applied between the anode 98 and the cathode 106, carriers including electrons and holes are injected though the hole injection layer and the electron injection layer. Such carriers are transported to a light emission layer (not shown) formed between the hole transport layer and the electron transport layer through the hole transport layer and the electron transport layer. At this moment, the hole transport layer and the electron transport layer transport the carriers to a light emission material to increase a probability of light emission combination within the light emission layer. If the carriers are injected, excitons are generated within the light emission layer, and the generated excitons emit the light corresponding to a polaron energy gap to become extinct. Herein, the generated light is radiated toward the insulating substrate 1 through the low refractive thin film 68 and the third insulating layer 94.

In the organic EL display panel with such a configuration, the light emitted from the light emission layer of the organic EL layer 104 is radiated through the insulating substrate 1 on which the low refractive thin film is spread, thus a light emission efficiency is improved as well as a brightness.

FIG. 9A to 9J are sectional diagrams representing a fabricating method of the active matrix organic EL display panel shown in FIG. 8 step by step. Each pattern in such a fabricating method is formed by way of going through a series of processes where a pattern drawn in a separate mask is formed by way of being transferred to a substrate on which a thin film is deposited. Such processes are photolithography including photo-resist coating, aligning & exposure and developing.

Referring to FIG. 9A to 9J, a low refractive thin film 68 is formed on the entire surface of an insulating substrate 1 as shown in FIG. 9A. The low refractive thin film 68 reduces the rate that the light generated from the organic EL diode E is refracted, thus the efficiency of the light emitted from the lower surface of the insulating

substrate 1 is improved. Such a low refractive thin film 68 is formed of a material with low refractive rate, e.g., mainly silica acrogel and silica gel.

Then, a buffer layer 70, an active layer 72a and a capacitor electrode 74, as shown in FIG. 9B, are formed on the insulating substrate 1 shown in FIG. 9A. At this moment, the buffer layer 70 is formed across the entire surface of the substrate in use of a first insulating material, and the active layer 72a and the capacitor electrode 74 are formed by a first mask process after depositing polycrystalline silicon on the upper part of the buffer 70.

Then, a gate insulating film 76 and a gate electrode 78, as shown in FIG. 9C, are formed at the central area of the active layer 72a. The gate insulating film 76 and the gate electrode 78 are formed by a second mask process after continuously depositing a second insulating material and a first metal material on the insulating substrate 1, as shown in FIG. 9B.

After forming the gate insulating film 76 and the gate electrode 78, as shown in FIG. 9D, an insulating layer 80 and a power electrode 82 are formed on the insulating substrate 1. The first insulating layer 80 is formed by way of spreading a third insulating material on the entire surface of the insulating substrate 1 shown in FIG 9C. The power electrode 82 is formed by way of patterning by a third mask process to cover the capacitor electrode 74 after depositing a second metal material on the upper part of the first insulating layer 80.

Then, a second insulating layer 84, as shown in FIG. 9E, is formed on the insulating substrate 1 shown in FIG 9D. The second insulating layer 84 is formed by way of patterning by a fourth mask process after depositing a third insulating material on the insulating substrate 1 shown in FIG 9D. Then, the second insulating layer 84 exposes both ends of the active layer 72a and a part of the power electrode 82 to have first and second ohmic contact holes 86a and 86b and a capacitor contact hole 88. Herein, both ends of the active layer 72a are connected through the first and second ohmic contact holes 86a and 86b and the source and drain electrodes formed in the following process. The left end of the active layer 72a becomes a drain area Ia, and the right end becomes a source area Ib.

The both exposed ends of the active layer 72a are ion-doped to become the ohmic contact layer 72b containing contains impurities. Hereby, the semiconductor layer 72 is completed, which includes the active layer 72a and the ohmic contact layer 72b.

After completion of the semiconductor layer 72, as

shown in FIG. 9F, the source and drain electrodes 90 and 92 are formed. The source and drain electrodes are formed by a fifth mask process after depositing a third metal material on the entire surface of the insulating substrate 1 shown in FIG. 9E. At this moment, the source electrode 90 is formed to be connected to the power electrode 82 and the ohmic contact layer 72b of the source area Ib through the first ohmic contact hole (86a of FIG. 9E) and the capacitor contact hole (88 of FIG. 9E), and the drain electrode 92 is formed to be connected to the ohmic contact layer 72b of the drain area Ia through the second ohmic contact hole (86b of FIG. 9E).

Through this process, the TFT T is completed, which includes the semiconductor layer 72, the gate electrode 78, the source and drain electrodes 90 and 92, and the storage capacitor Cst is formed at a corresponding area between the power electrode 82 and the capacitor electrode 74. Even though not shown in the drawings, the capacitor electrode 74 is connected to the gate electrode 78, the power electrode 82 is formed to be unified with the power supply line located to be parallel to the signal line.

Then, the third insulating layer 94, as shown in FIG. 9G, is formed. The third insulating layer 94 is formed by way of patterning by a sixth mask process to form the drain contact hole 96 after depositing a fourth insulating material on the entire surface of the insulating substrate 1 shown in FIG. 9F.

Then, an anode 98, as shown in FIG. 9H, is formed on the light emission area I. The anode 98 is formed by an seventh mask process in use of a transparent conductive material to be connected to the drain electrode 92 through the drain contact hole (96 of FIG. 9G).

Then a protective layer 100 is formed to have an anode-exposed part 102 as shown in FIG. 9I. The protective layer 100 is formed by way of patterning by a eighth mask process to expose a part of the anode 98 after depositing a fifth insulating material on the insulating substrate 1 shown in FIG. 9H. Herein, the protective layer 100 acts to protect the TFT T from moisture and impurities.

Hereby, the mask process including the photolithography is completed, an organic EL layer 104 and a cathode 106 are sequentially formed, which forms an organic EL diode E along with the anode 98 through the anode-exposed part (102 of FIG. 9I) as shown in FIG. 9J.

In this way, the organic EL display panel according to the first to third embodiments of the present invention eliminates inorganic insulating layers and forms the low refractive thin film on the light emission area, so that the light emission efficiency can be improved as well as

brightness. Furthermore, the organic EL display panel and the fabricating method thereof according to the present invention can change the positions of the anode and the cathode in accordance with the characteristic of carriers supplied from the TFT T, and has the compensating TFTs added to the drive circuit shown in FIG. 1 to improve brightness uniformity, thus a method of being configured with four TFTs can be applied.

[Effect of the Invention]

As described above, the active matrix organic EL display panel and the fabricating method thereof according to the present invention has the low refractive thin film formed on the substrate and, in addition, can eliminate insulating films of inorganic insulating material on the light emission area through the fabricating process of the thin film transistor. Due to this, the active matrix organic EL display panel according to the present invention radiates the light emitted from the organic EL diode to the lower substrate and, in addition, uses the low refractive material, so that light emission efficiency can be improved as well as brightness.

Although the present invention has been explained by the embodiments shown in the drawings described above, it should be understood to the ordinary skilled person in the art that the invention is not limited to the embodiments, but rather that various changes or modifications thereof are possible without departing from the spirit of the invention. Accordingly, the scope of the invention shall be determined only by the appended claims and their equivalents.

[What is claimed is:]

1. An active matrix type organic electro luminescence display panel comprising:

a substrate having a defined light emission area;

a low refractive thin film, made of a low refractive material on the substrate, reducing a loss of light;

thin film transistors, formed on a predetermined location of the substrate having the low refraction thin film by a mask process having a photolithography method, switching and driving by a control signal from an exterior;

a storage capacitor connected to the thin film transistor to charge/discharge a data signal from the exterior; and

an organic electro luminescence diode, patterned by the mask process of the thin film transistors to be formed on the substrate, which the light emission area is exposed, emitting light by an exterior current and voltage.

2. The active matrix type organic electro luminescence display panel according to claim 1, wherein the low refractive thin film is patterned by the mask process of the thin film transistors to expose the substrate having the light emission area, and then is included in between the insulated substrate and the organic electro luminescence diode.

3. The active matrix type organic electro luminescence display panel according to claim 2, wherein the low refractive material has a refractive rate (n) less than 1.5.

4. The active matrix type organic electro luminescence display panel according to claim 3, wherein the low refractive material includes silica aerogel and silica gel, which have a refractive rate (n) less than 1.5.

5. The active matrix type organic electro luminescence display panel according to claim 4, wherein the silica aerogel has a refractive rate n of about 1.07.

6. The active matrix type organic electro luminescence display panel according to claim 1, wherein the organic electro luminescence diode includes:

a first electrode formed of a transparent conductive material on the light emission area of the substrate;

an organic light emission layer formed of an organic light emission material on the light emission area of the substrate to cover the first electrode; and

a second electrode formed of a metal material on an upper part of the organic light emission layer to coat the entire surface of the substrate.

7. The active matrix type organic electro luminescence display panel according to claim 6, wherein the thin film transistors includes:

a semiconductor layer formed on the substrate;

a gate insulating film and a gate electrode stacked sequentially on an upper part of the semiconductor layer;

a drain electrode formed to be connected to the semiconductor layer and the first electrode of the organic electro luminescence diode; and

a source electrode simultaneously formed together with the drain electrode to be connected to the semiconductor layer and the storage capacitor.

8. The active matrix type organic electro luminescence display panel according to claim 7, wherein the storage capacitor includes:

a capacitor electrode separated from the semiconductor layer by a predetermined distance on the substrate; and

a power electrode insulated from an upper part of the capacitor electrode and then connected to the source electrode, as well as, formed to cover the capacitor electrode.

9. The active matrix type organic electro luminescence display panel according to claim 7, wherein the semiconductor layer is a P type semiconductor layer, and the first and the second electrodes are an anode and a cathode, respectively.

10. The active matrix type organic electro luminescence display panel according to claim 6, wherein the transparent conductive material includes indium-tin-oxide (ITO).

11. An active matrix type organic electro luminescence display panel comprising:

a substrate having a defined light emission area;

a low refractive thin film formed by applying a low refractive material to the substrate in order to reduce a loss of the emitting light;

thin film transistors, formed on a predetermined location of the substrate by a mask process having a photolithography method, switching and driving by a control signal from an exterior;

a storage capacitor connected to the thin film

transistor to charge/discharge a data signal from the exterior; and

an organic electro luminescence diode formed on the light emission area of the substrate having the thin film transistor and the storage capacitor, and emitting light by an external current and a voltage.

12. The active matrix type organic electro luminescence display panel according to claim 11, wherein the low refractive material has a refractive rate (n) less than 1.5.

13. The active matrix type organic electro luminescence display panel according to claim 12, wherein the low refractive material includes silica aerogel and silica gel, which have a refractive rate (n) less than 1.5.

14. The active matrix type organic electro luminescence display panel according to claim 13, wherein the silica aerogel has a refractive rate n of about 1.07.

15. The active matrix type organic electro luminescence display panel according to claim 11, wherein the organic electro luminescence diode includes:

a first electrode formed of a transparent conductive material on the light emission area of the substrate;

an organic light emission layer formed of an organic light emission material on the light emission area of the substrate to cover the first electrode; and

a second electrode formed of a metal material on an upper part of the organic light emission layer to coat the entire surface of the substrate.

16. The active matrix type organic electro luminescence display panel according to claim 15, wherein the thin film transistors includes:

a semiconductor layer formed on the substrate;

a gate insulating film and a gate electrode stacked sequentially on an upper part of the semiconductor layer;

a drain electrode formed to be connected to the semiconductor layer and the first electrode of the organic electro luminescence diode; and

a source electrode simultaneously formed together with the drain electrode to be connected to the semiconductor layer and the storage capacitor.

17. The active matrix type organic electro luminescence display panel according to claim 16, wherein the storage capacitor includes:

a capacitor electrode separated from the

semiconductor layer by a predetermined distance on the substrate; and

a power electrode insulated from an upper part of the capacitor electrode and then connected to the source electrode, as well as, formed to cover the capacitor electrode.

18. The active matrix type organic electro luminescence display panel according to claim 16, wherein the semiconductor layer is a P type semiconductor layer, and the first and the second electrodes are an anode and a cathode, respectively.

19. The active matrix type organic electro luminescence display panel according to claim 15, wherein the transparent conductive material includes indium-tin-oxide (ITO).

20. A method of fabricating an active matrix type organic electro luminescence display panel comprising:

forming a low refractive thin film by applying a low refractive material on the entire surface of a substrate having a defined light emission area;

forming a buffer layer on the substrate having the low refractive thin film by way of a mask process to reveal the light emission area on the substrate;

forming an active layer and a capacitor electrode separated by a predetermined distance from each other on the buffer layer by way of a mask process having exposing, developing, and etching;

sequentially forming a gate insulating film and a gate electrode at a central part of the active layer;

forming a first insulating layer on the entire surface of the substrate to cover the gate insulating film and the gate electrode;

forming a power electrode on the substrate to cover an area corresponding to the capacitor electrode of the first insulating layer;

forming a second insulating layer on the entire surface of the substrate to cover the power electrode;

exposing the substrate onto which the low refractive thin film on a predetermined area of the active layer and the power electrode and the light emission area is coated;

ion-doping the substrate having the exposed active layer to complete a semiconductor layer;

forming a source electrode and a drain electrode separated by a predetermined distance from each other through a predetermined area of the semiconductor layer and the power electrode;

forming a third insulating layer to cover the source

and the drain electrodes;

forming a drain contact hole and patterning the third insulating layer to expose the substrate onto which the low refractive thin film of the light emission area is coated; and

forming an organic electro luminescence diode connected to the drain electrode on the substrate, which the exposed low refractive thin film of the light emission area is coated.

21. The method according to claim 20, wherein the low refractive material includes at least one of silica aerogel and silica gel, which have a refractive rate n less than 1.5.

22. The method according to claim 20, wherein the forming the organic electrode luminescence diode includes:

forming a first electrode made of a transparent conductive material on the emission area having the substrate onto which the exposed low refractive thin film is coated;

applying an organic light emission material to the light emission area having the first electrode to form an organic light emission layer; and

forming a second electrode made of a metal material on the entire surface of the substrate to apply an electrical signal to the organic light emission layer together with the first electrode.

23. The method according to claim 22, further comprising forming a protective layer, which a light emission part of the first electrode is exposed, after forming the first electrode.

24. The method according to claim 22, wherein the semiconductor layer is a P type semiconductor layer doped by a P type ion, and the first and the second electrode are respectively an anode and a cathode.

25. The method according to claim 22, wherein the transparent conductive material includes indium-tin-oxide (ITO).

26. A method for fabricating an active matrix type organic luminescence display panel comprising:

forming a buffer layer on the substrate having a defined light emission area by way of a mask process to reveal the light emission area;

forming an active layer and a capacitor electrode separated by a predetermined distance from each other on

the buffer layer by way of a mask process having exposing, developing, and etching;

sequentially forming a gate insulating film and a gate electrode at a central part of the active layer;

forming a first insulating layer on the entire surface of the substrate to cover the gate insulating film and the gate electrode;

forming a power electrode on the substrate to cover an area corresponding to the capacitor electrode of the first insulating layer;

forming a second insulating layer on the entire surface of the substrate to cover the power electrode;

exposing the substrate onto which the low refractive thin film on a predetermined area of the active layer and the power electrode and the light emission area is coated;

ion-doping the substrate having the exposed active layer to complete a semiconductor layer;

forming a source electrode and a drain electrode separated by a predetermined distance from each other through a predetermined area of the semiconductor layer and the power electrode;

sequentially forming a third insulating layer and a low refractive thin film to cover the source and the drain electrodes;

patterning the third insulating layer and the low refractive thin film so as to form a drain contact hole; and

forming an organic electro luminescence diode connected to the drain electrode on the substrate, which the exposed low refractive thin film of the light emission area is coated.

27. The method according to claim 26, wherein the low refractive thin film is formed of a low refractive material, wherein the low refractive material includes at least one of silica aerogel and silica gel, which have a refractive rate n less than 1.5.

28. The method according to claim 26, wherein the forming the organic electrode luminescence diode includes:

forming a first electrode of a transparent conductive material on the emission area having the substrate to which the third insulating layer and the low refractive thin film are sequentially stacked;

applying an organic light emission material to the light emission area having the first electrode to form an organic light emission layer; and

forming a second electrode of a metal material on the entire surface of the substrate to apply an electrical signal to the organic light emission layer together with

the first electrode.

29. The method according to claim 28, further comprising forming a protective layer which a light emission part of the first electrode is exposed, after forming the first electrode.

30. The method according to claim 26, wherein the semiconductor layer is a P type semiconductor layer doped by a P type ion, and the first and the second electrode are respectively an anode and a cathode.

31. The method according to claim 28, wherein the transparent conductive material includes indium-tin-oxide (ITO).

32. A method of fabricating an active matrix type organic electro luminescence display panel comprising:

forming a low refractive thin film by applying a low refractive material to the entire surface of a substrate having a defined light emission area;

forming a buffer layer on the entire surface of the substrate having the low refractive thin film;

forming an active layer and a capacitor electrode separated by a predetermined distance from each other on the buffer layer by way of a mask process having exposing, developing, and etching;

sequentially forming a gate insulating film and a gate electrode at a central part of the active layer;

forming a first insulating layer on the entire surface of the substrate to cover the gate insulating film and the gate electrode;

forming a power electrode on the substrate to cover an area corresponding to the capacitor electrode of the first insulating layer;

forming a second insulating layer on the entire surface of the substrate to cover the power electrode;

exposing a predetermined area of the active layer and the power electrode;

ion-doping the substrate having the exposed active layer to complete a semiconductor layer;

forming a source electrode and a drain electrode separated by a predetermined distance from each other through a predetermined area of the semiconductor layer and the power electrode;

forming a third insulating layer to cover the source and the drain electrodes;

patterning the third insulating layer so as to form a drain contact hole; and

forming an organic electro luminescence diode on the

substrate so as to connect to the drain electrode.

33. The method according to claim 32, wherein the low refractive material includes at least one of silica aerogel and silica gel, which have a refractive rate n less than 1.5.

34. The method according to claim 32, wherein the forming the organic electrode luminescence diode includes:

forming a first electrode of a transparent conductive material on the emission area having the substrate to which the low refractive thin film, the buffer layer, and the first to the third insulating layer are sequentially stacked;

applying an organic light emission material to the light emission area of the substrate having the first electrode to form an organic light emission layer; and

forming a second electrode of a metal material on the entire surface of the substrate to apply an electrical signal to the organic light emission layer together with the first electrode.

35. The method according to claim 34, further comprising forming a protective layer, which a light emission part of the first electrode is exposed, after forming the first electrode.

36. The method according to claim 32, wherein the semiconductor layer is a P type semiconductor layer doped by a P type ion, and the first and the second electrodes are respectively an anode and a cathode.

37. The method according to claim 34, wherein the transparent conductive material includes indium-tin-oxide (ITO).

FIG.1

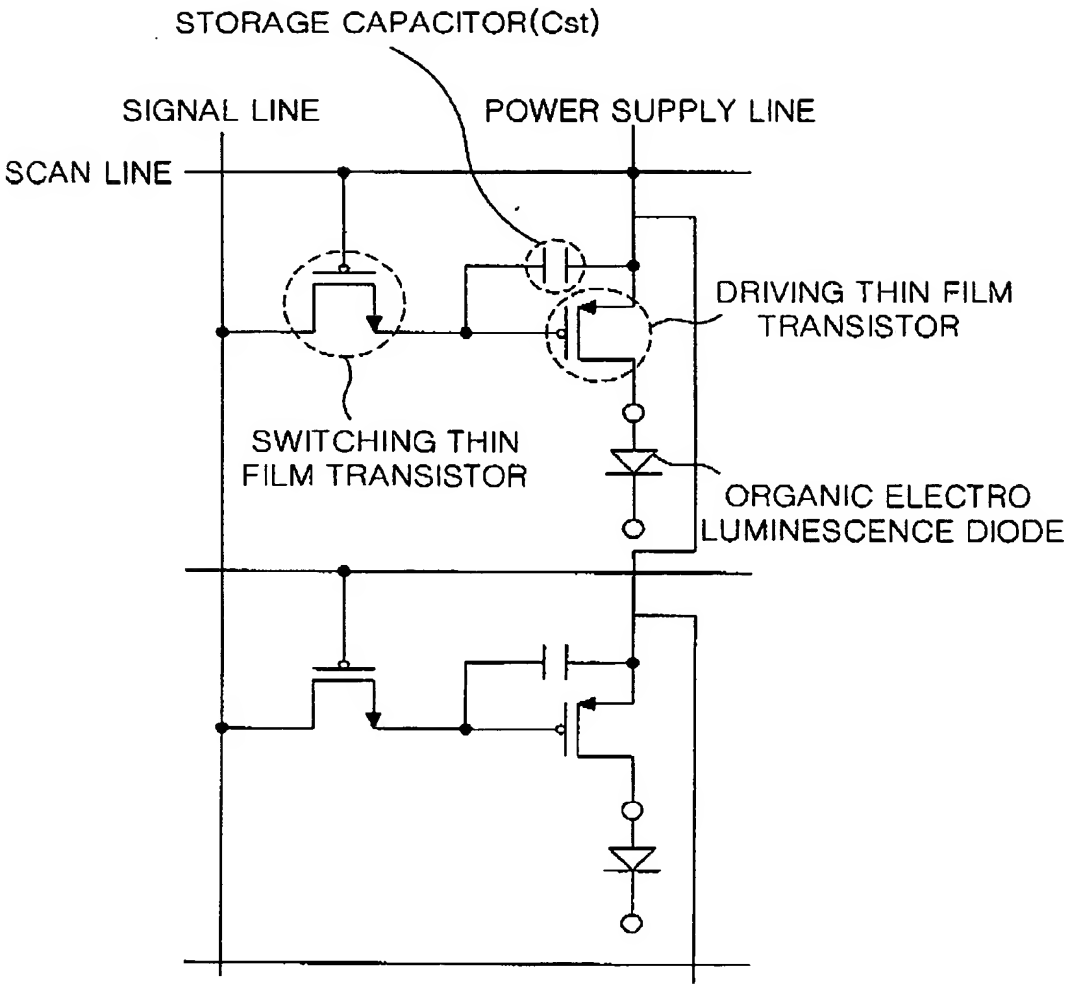

STORAGE CAPACITOR(Cst)
SIGNAL LINE
POWER SUPPLY LINE
SCAN LINE
DRIVING THIN FILM TRANSISTOR
SWITCHING THIN FILM TRANSISTOR
ORGANIC ELECTRO LUMINESCENCE DIODE

FIG.2

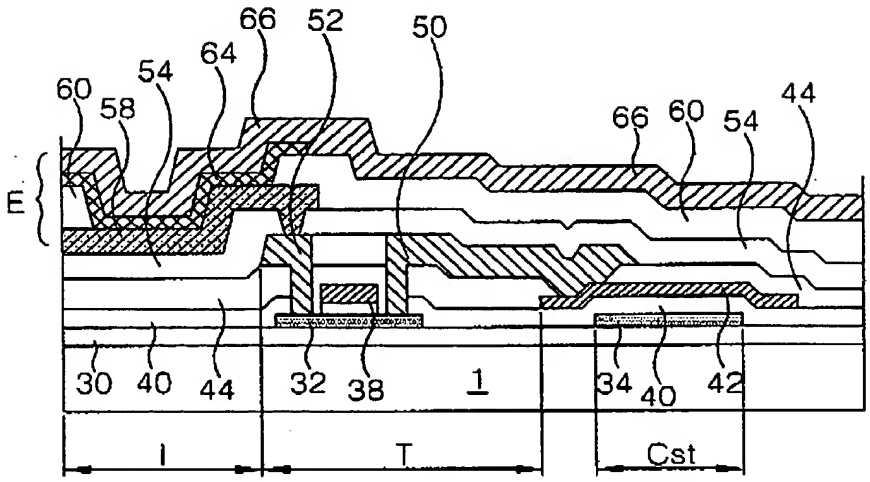


FIG.3A

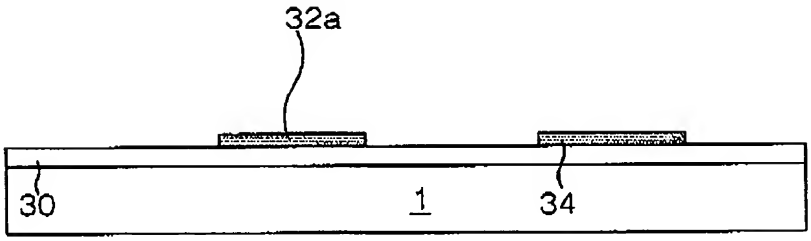


FIG.3B

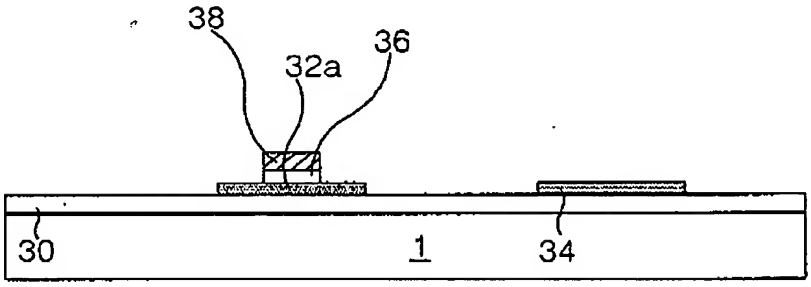


FIG.3C

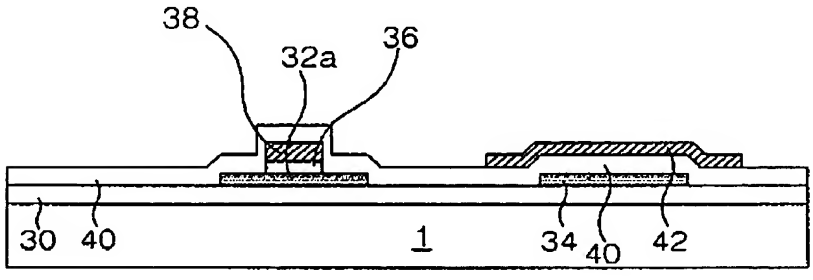


FIG.3D

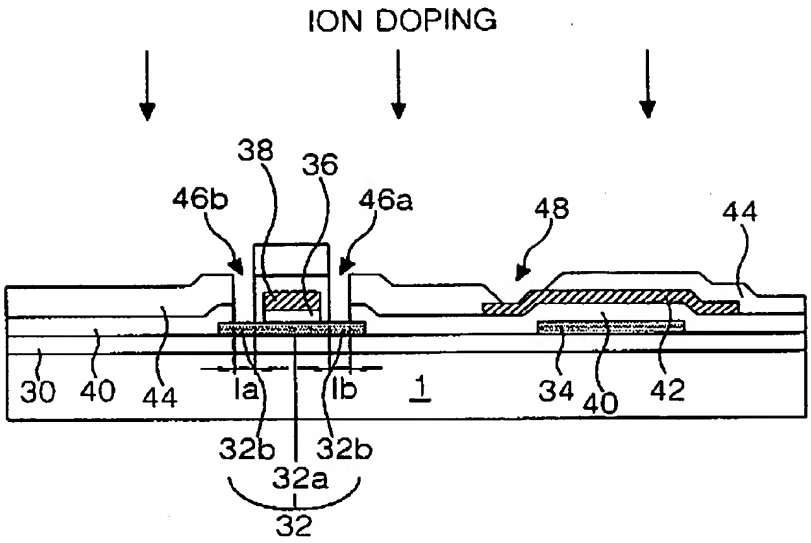
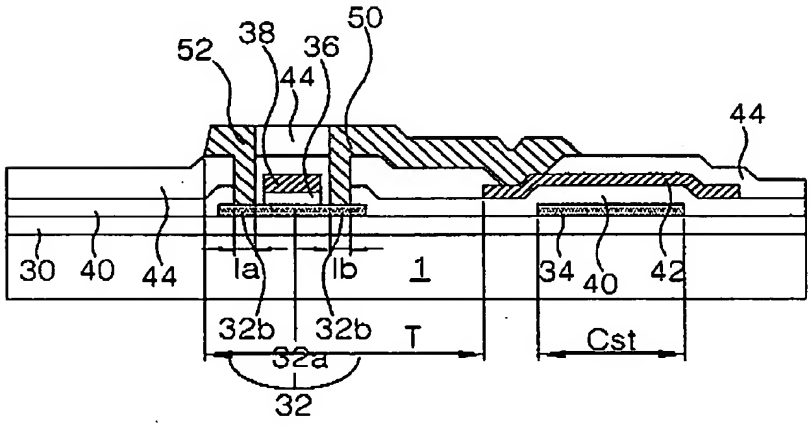

ION DOPING
38
36
46b
46a
48
44
30
40
44
1a
1b
1
34
40
42
32b
32b
32a
32

FIG.3E


52
38
36
50
44
44
30
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44
1a
1b
1
34
40
42
32b
32b
T
Cst
32a
32

FIG.3F

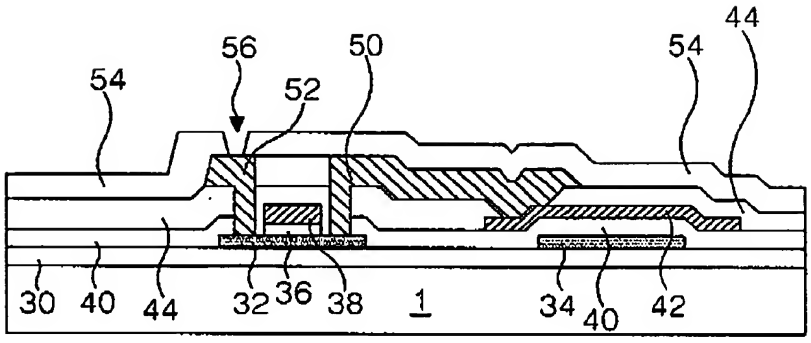
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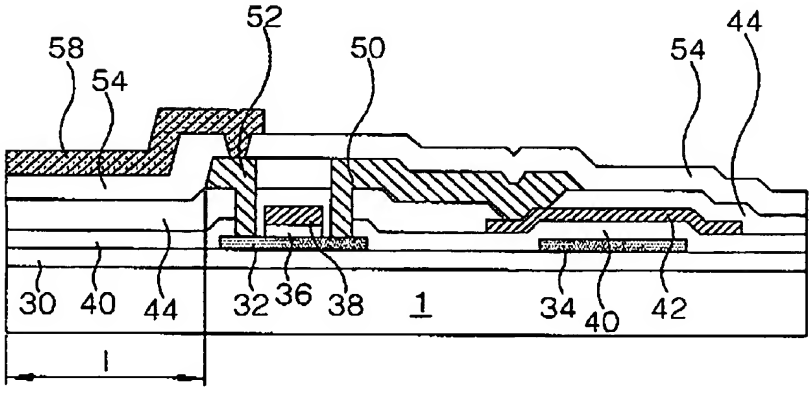
FIG.3G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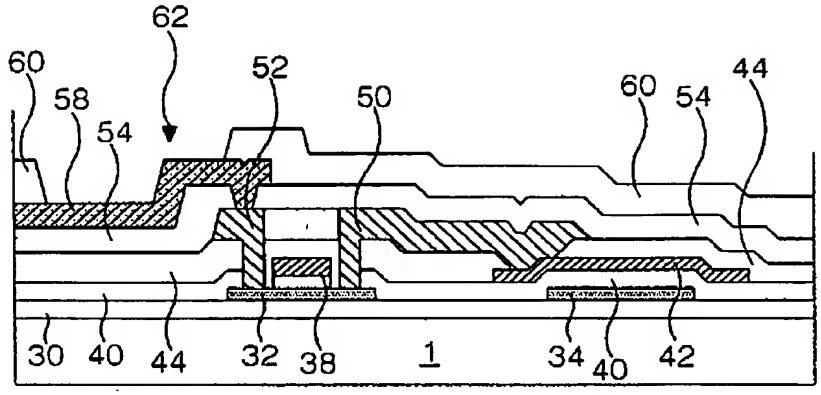
l

FIG.3H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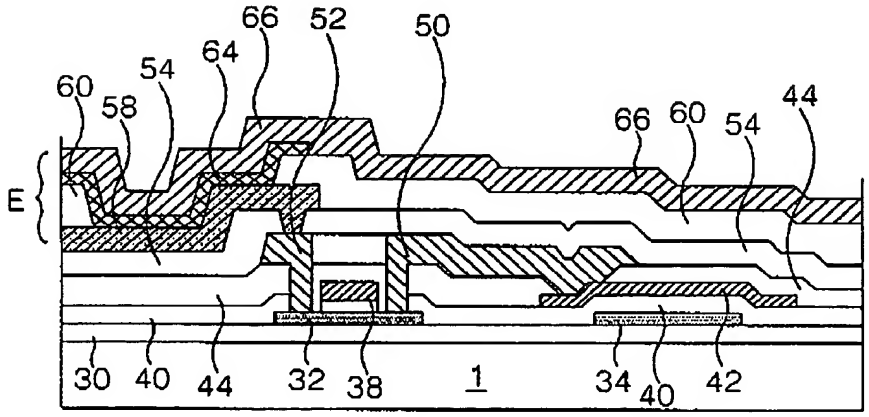
32
38
1
34
40
42

FIG.3I


66
52
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1
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40
42

FIG.4

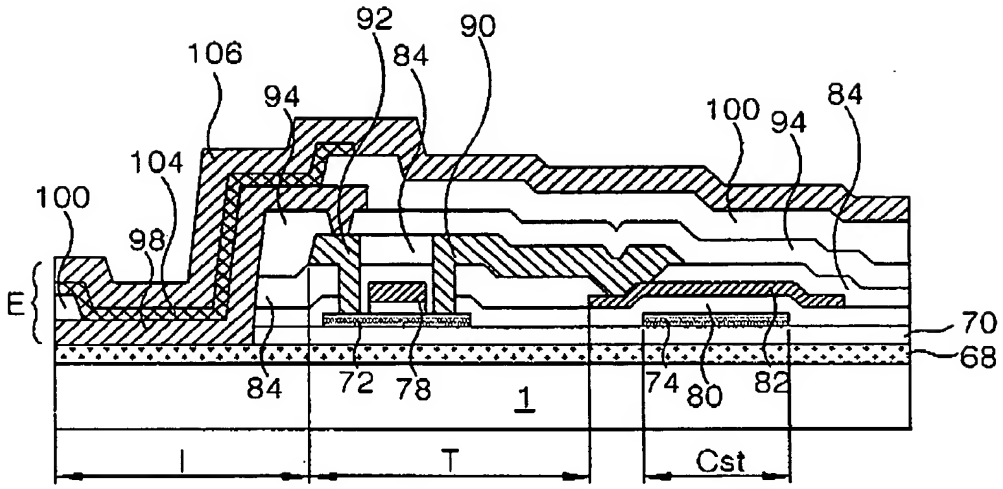


FIG.5A

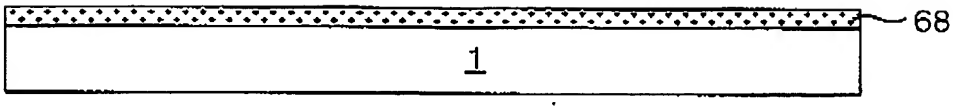


FIG.5B

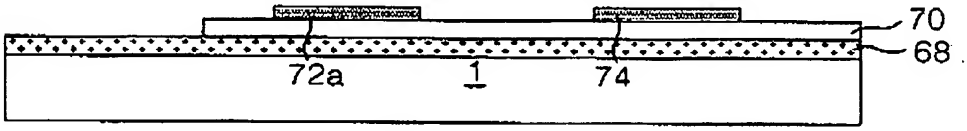


FIG.5C

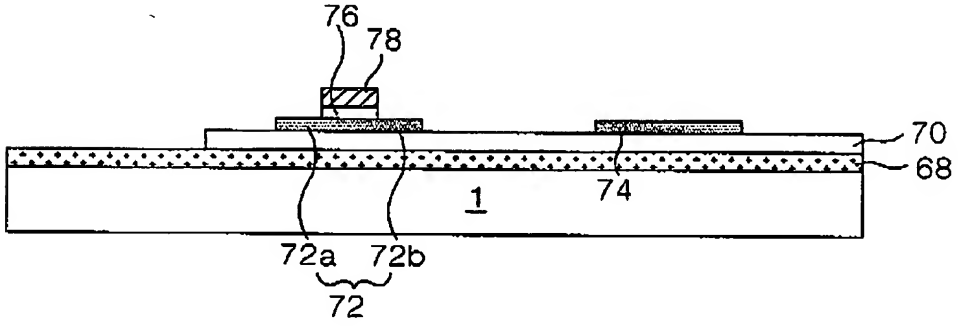


FIG.5D

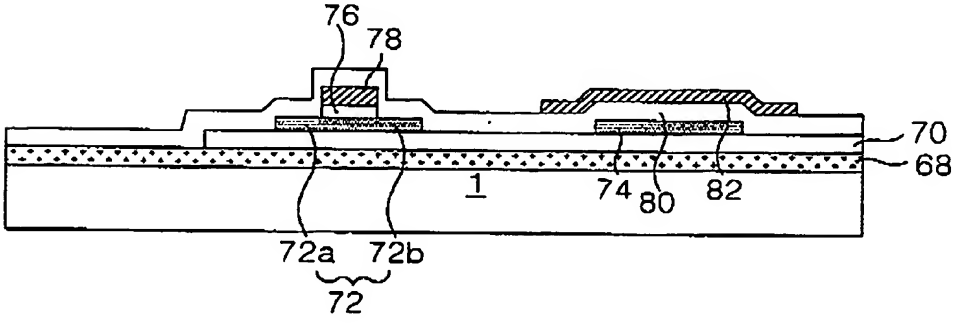
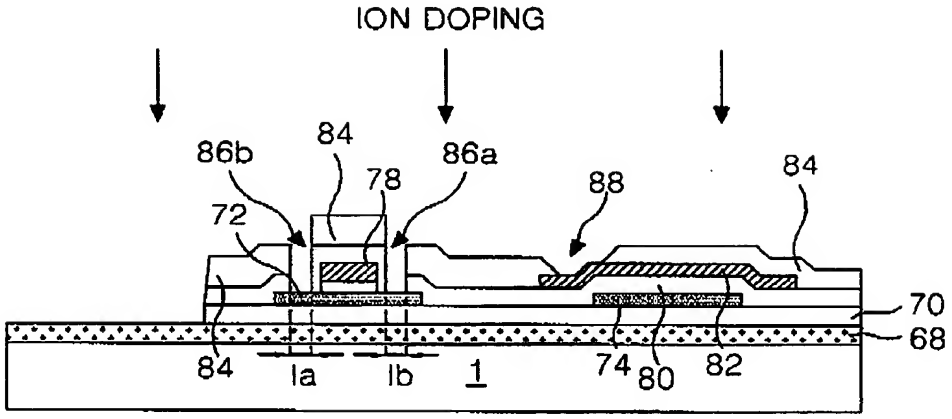


FIG.5E


ION DOPING
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Ia
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FIG.5F

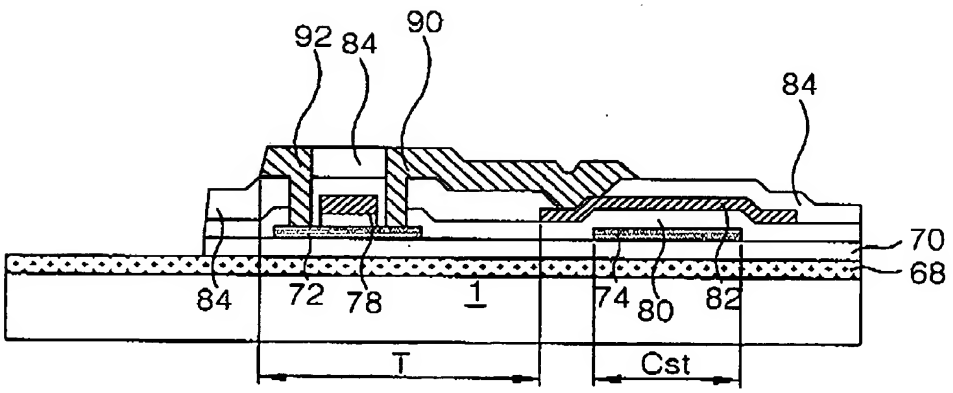
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FIG.5G

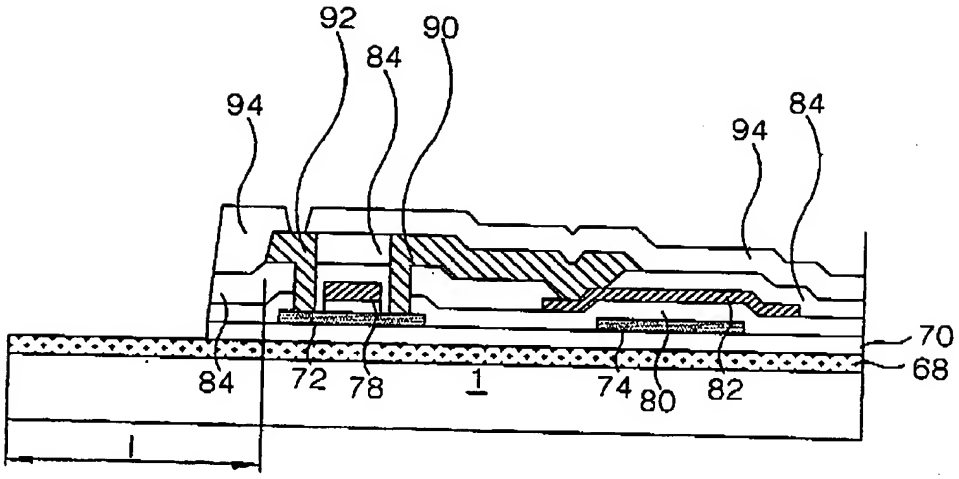
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FIG.5H

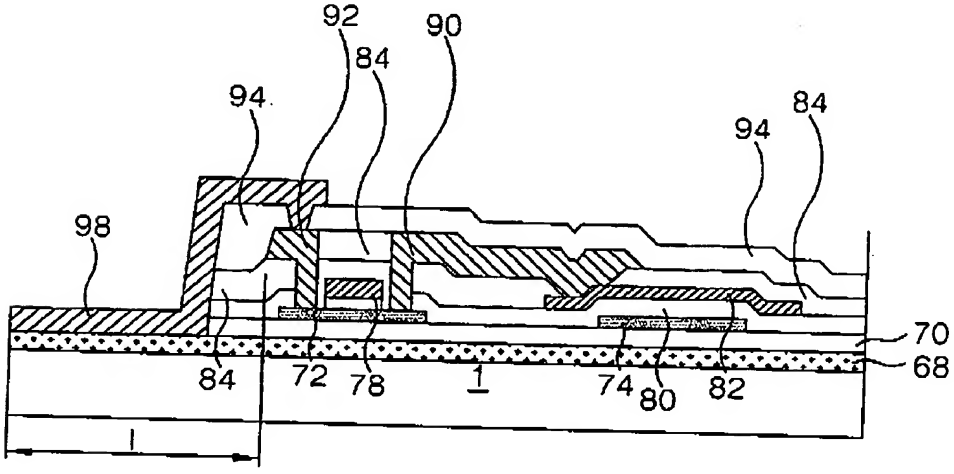
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FIG.5I

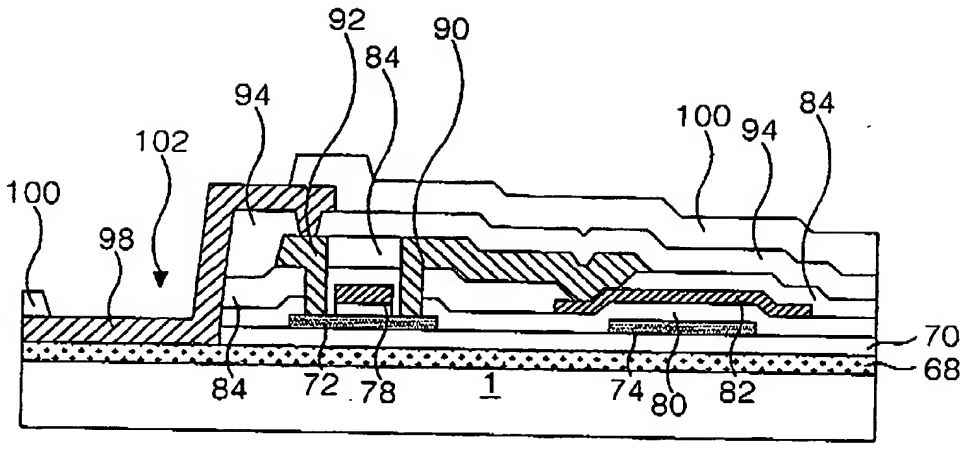
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FIG.5J

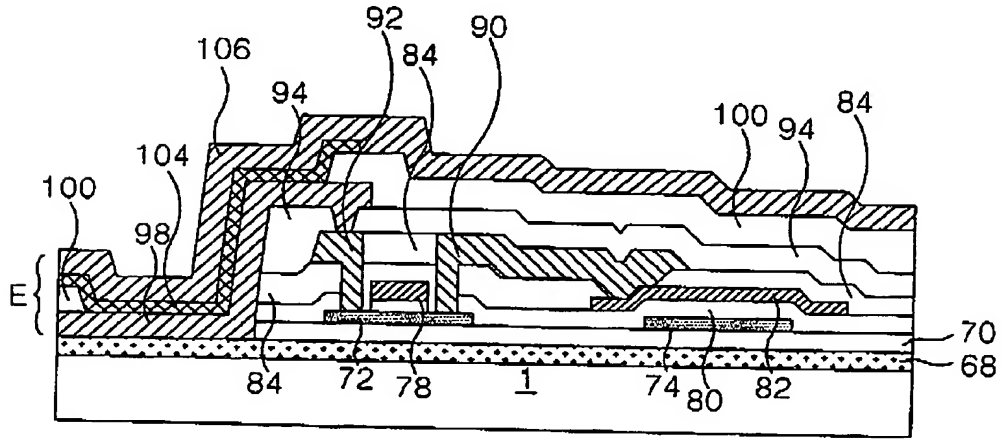
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FIG.6

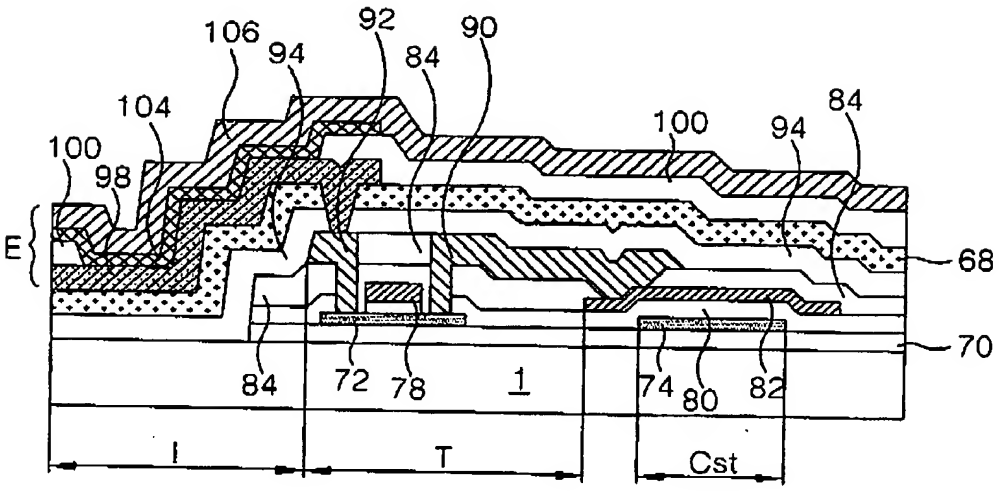

FIG.7A

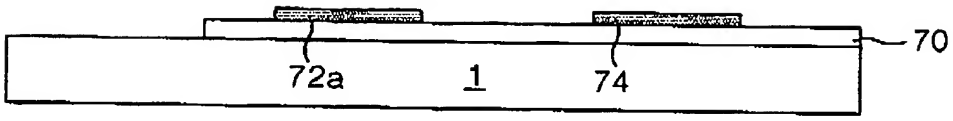

FIG.7B

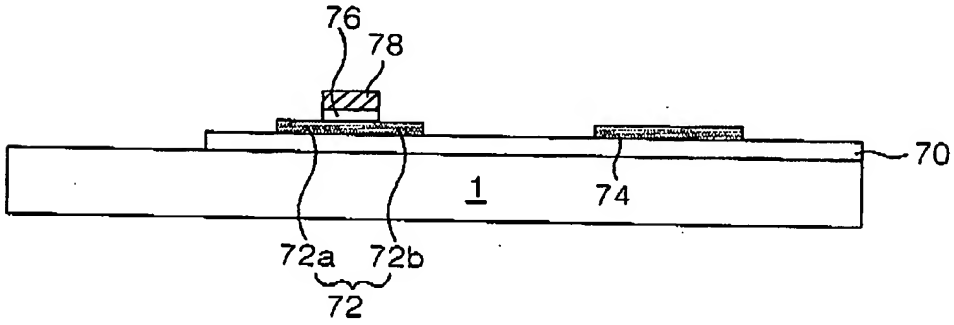

FIG.7C

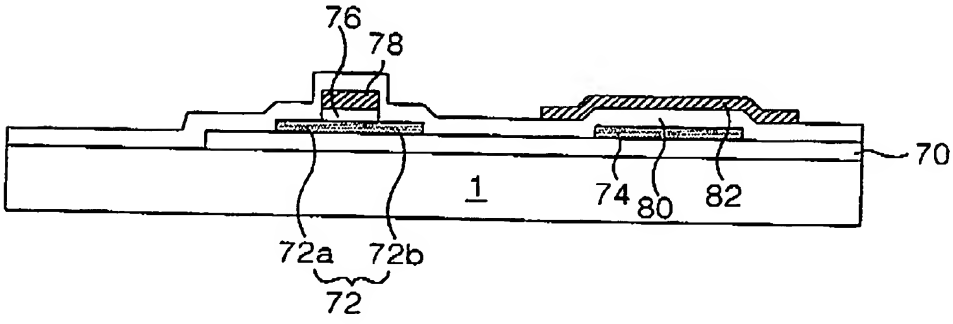

FIG.7D

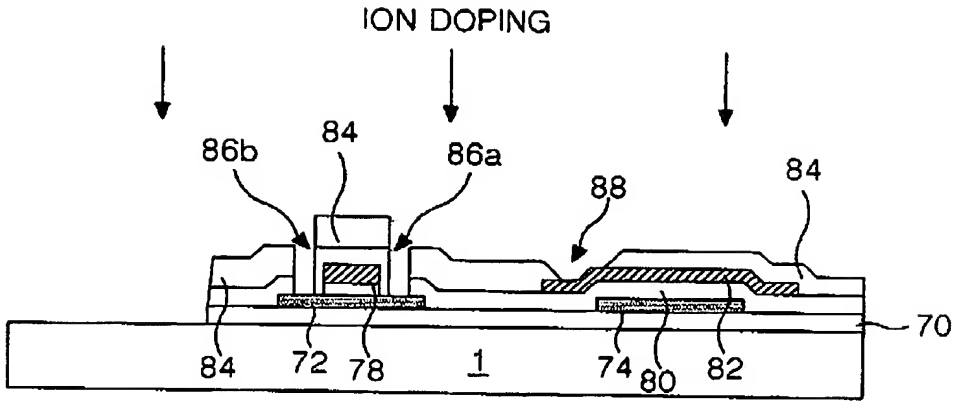
ION DOPING
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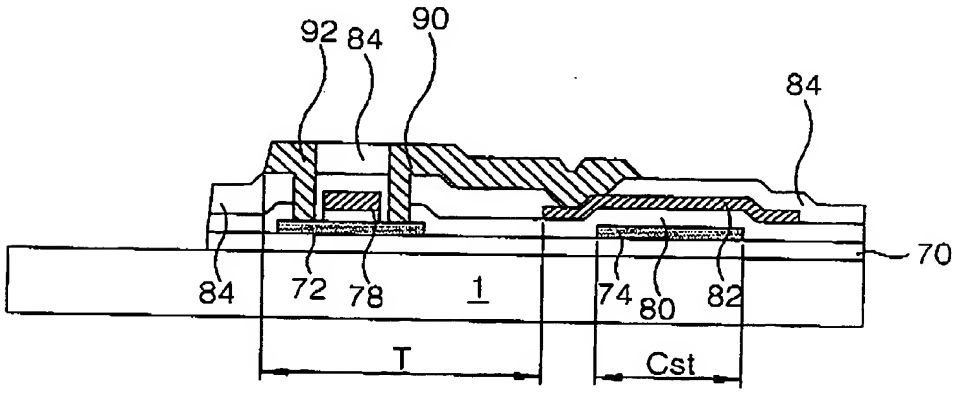
FIG.7E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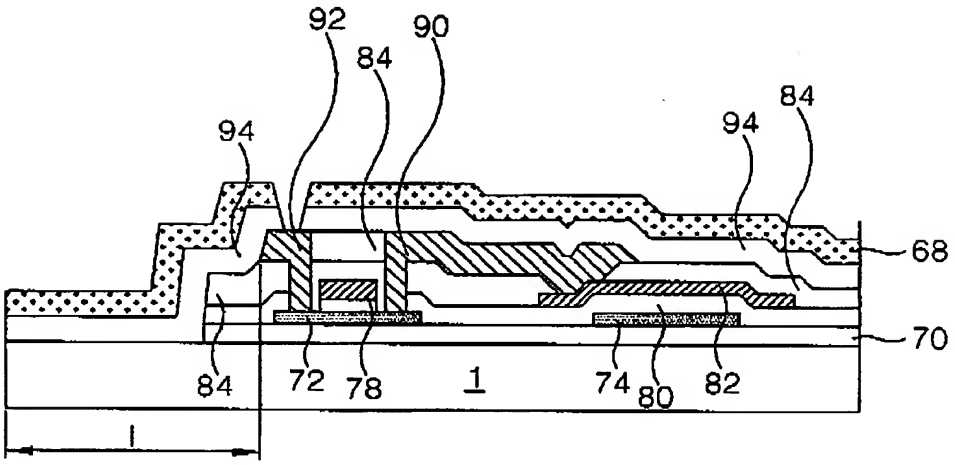
T
Cst

FIG.7F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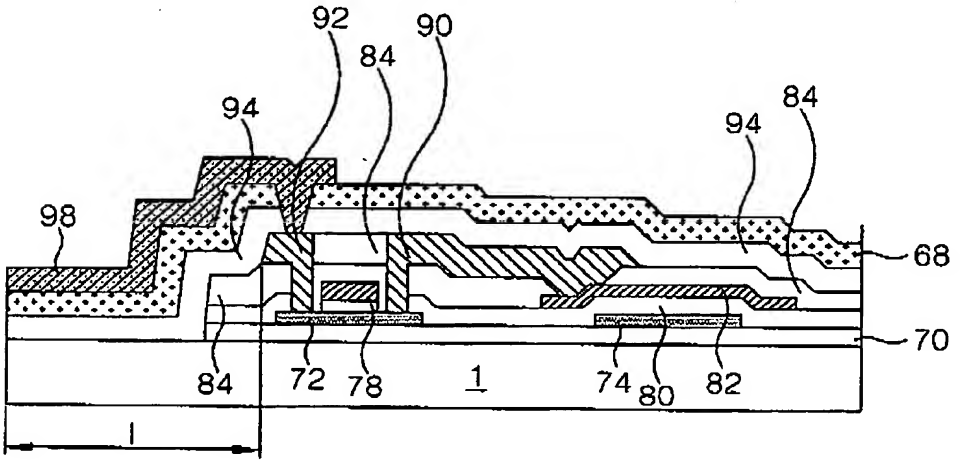
l

FIG.7G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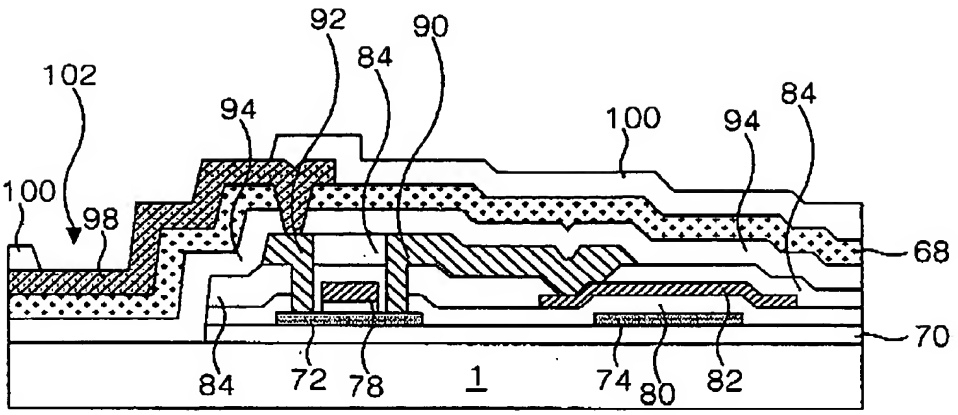
82
l

FIG.7H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100
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70
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72
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1
74
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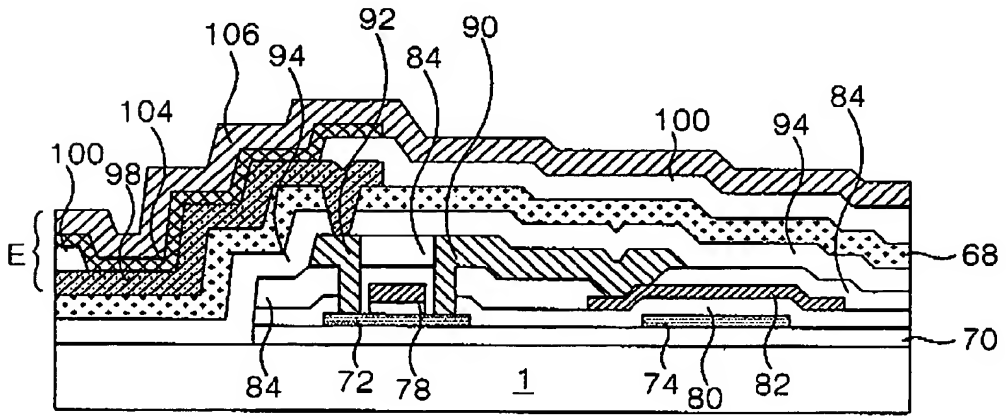
82

FIG.7I


106
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E
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1
74
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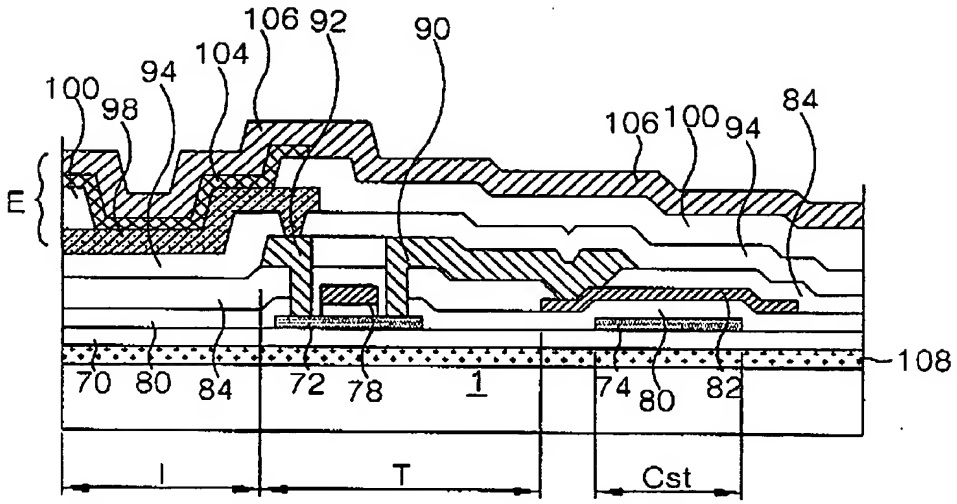
82

FIG.8


106
92
90
104
94
100
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E
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108
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1
74
80
82
I
T
Cst

FIG.9A

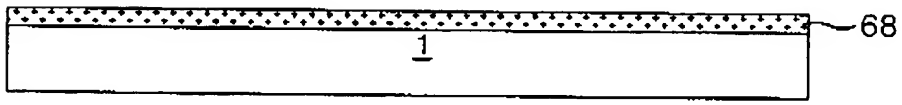

68
1

FIG.9B

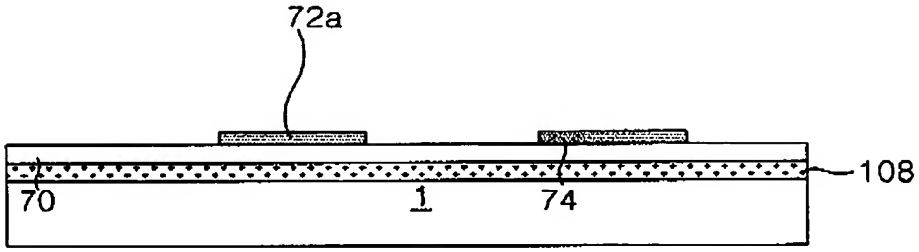


FIG.9C

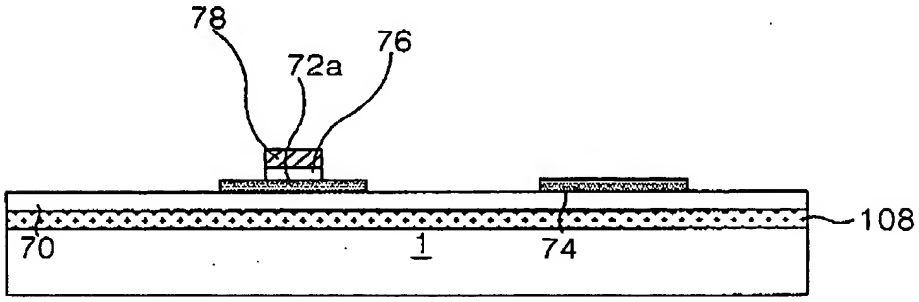


FIG.9D

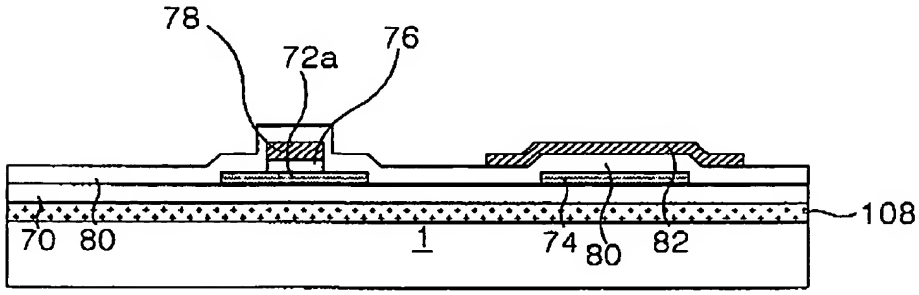
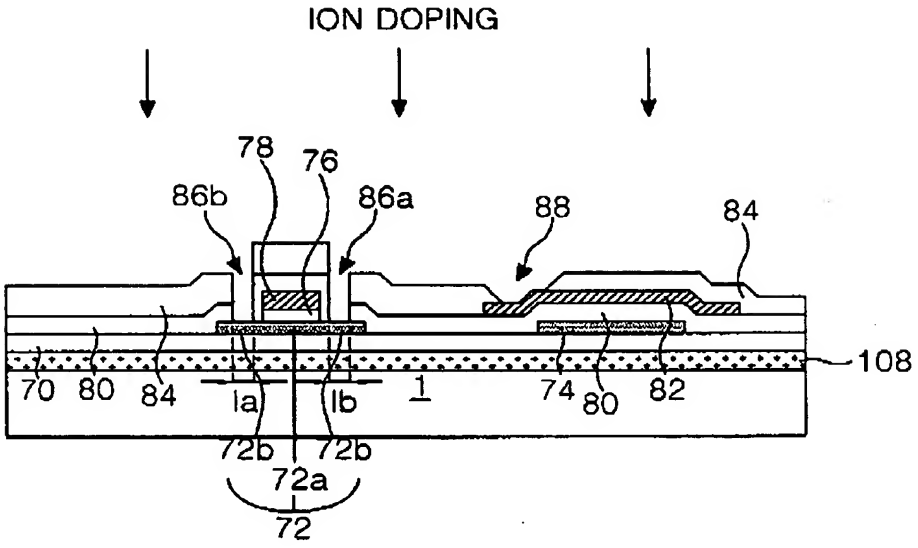


FIG.9E


ION DOPING
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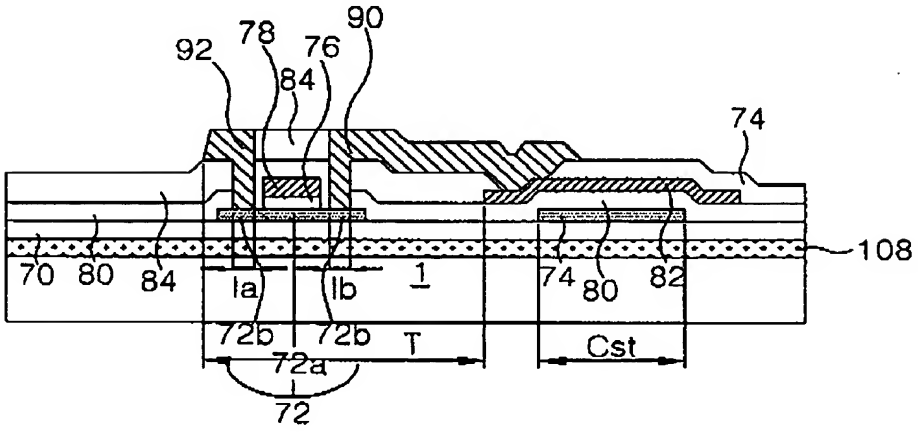
82
72b
72b
72a
72

FIG.9F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92
78
76
84
74
108
70
80
84
1a
1b
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74
80
82
72b
72b
T
Cst
72a
72

FIG.9G

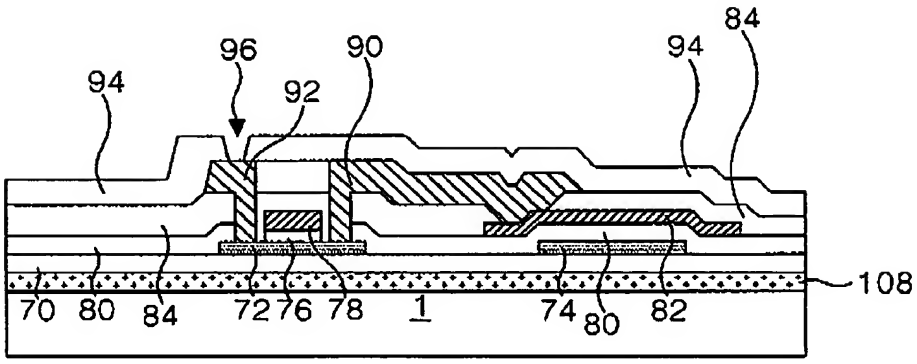

84
96
90
94
94
92
108
70
80
84
72
76
78
1
74
80
82

FIG.9H

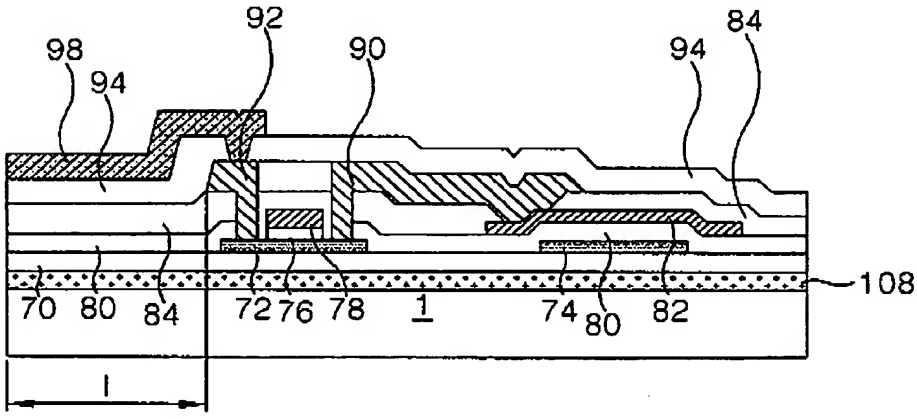
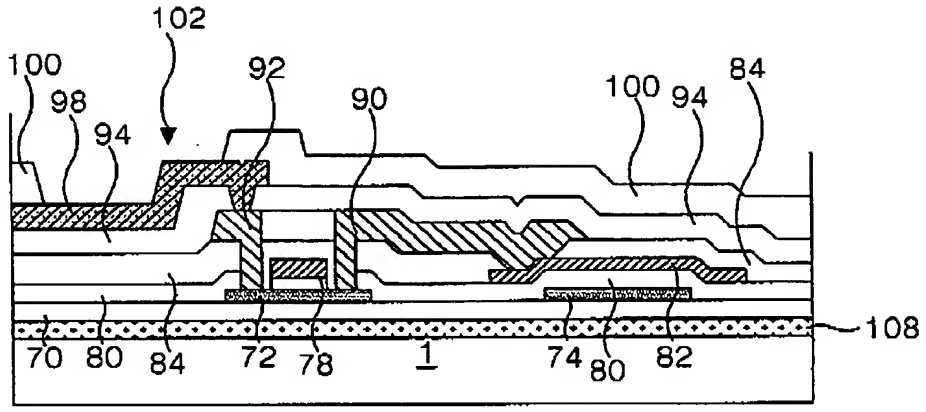

92
84
98
90
94
94
108
70
80
84
72
76
78
1
74
80
82
l

FIG.9I


102
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92
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100
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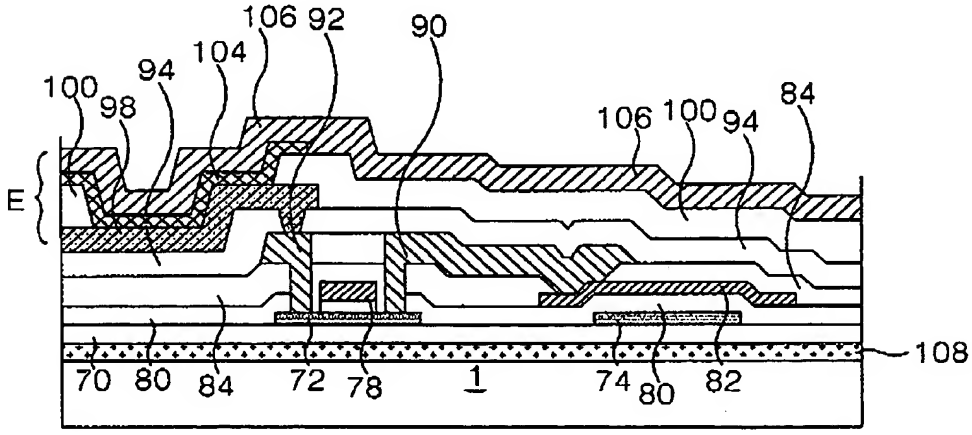
84
108
70
80
84
72
78
1
74
80
82

FIG.9J


106
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104
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100
98
106
100
94
84
E
108
70
80
84
72
78
1
74
80
82